

Memory FeRAM

256K (32K × 8) Bit SPI

MB85RS256LYA

■ DESCRIPTION

MB85RS256LYA is a FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 32,768 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. This product is specifically targeted for high-temperature environment such as automobile applications.

MB85RS256LYA adopts the Serial Peripheral Interface (SPI).

The MB85RS256LYA is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85RS256LYA can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E²PROM.

As MB85RS256LYA does not need any waiting time in writing process, the write cycle time of MB85RS256LYA is much shorter than that of Flash memories or E²PROM.

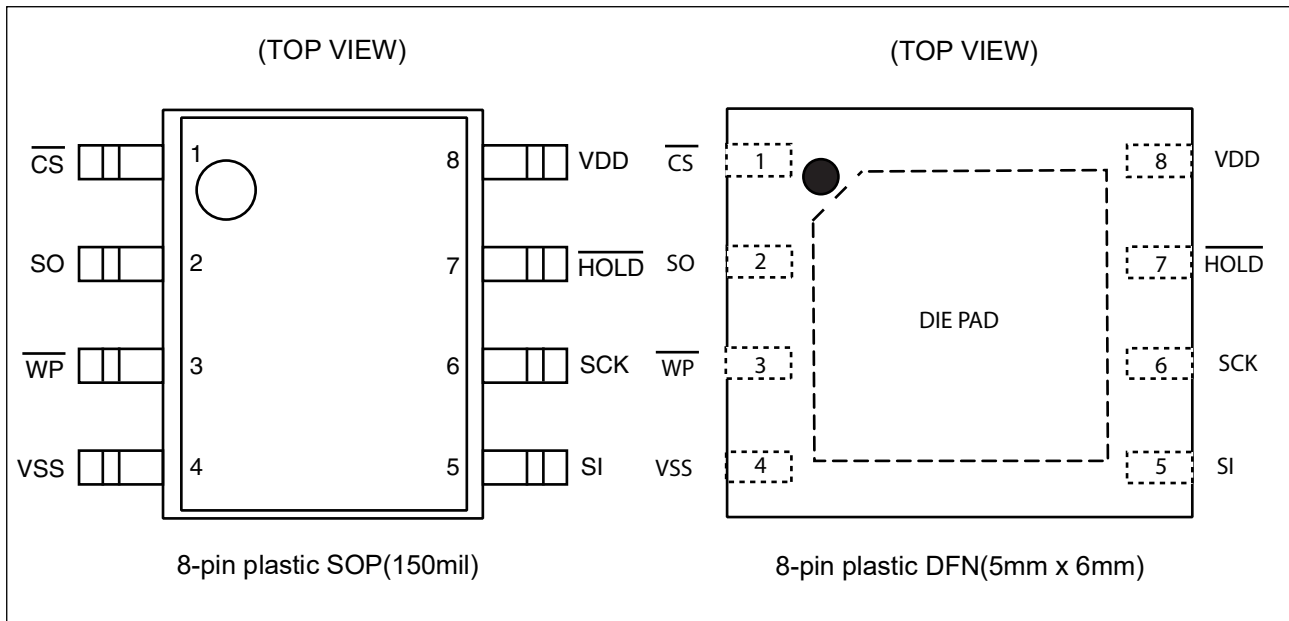
■ FEATURES

- Bit configuration : 32,768 words × 8 bits
- Special Sector Region : 256 words × 8 bits
In this region, data storage after (by) three times reflow based on JEDEC MSL-3 standard condition is guaranteed.
- Unique ID
- Serial Number : 64 bits
In this region, data storage after (by) three times reflow based on JEDEC MSL-3 standard condition is guaranteed.
- Serial Peripheral Interface : SPI (Serial Peripheral Interfaces)
Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 50 MHz (Max)
- High endurance : 10^{13} times(+125 °C), 10^{14} times (+85 °C)
- Data retention : 193.9 years (+85 °C)
40.7 years (+105 °C)
10.1 years (+125 °C) or more
Under evaluation for more than 10.1 years(+125 °C)
- Operating power supply voltage : 1.7 V to 1.95 V
- Low power consumption : Operating power supply current 3.0mA (Max@50 MHz)
Standby current 150μA (Max)
- Operation ambient temperature range : - 40 °C to +125 °C
- Package : 8-pin plastic SOP (150mil)
8-pin plastic DFN (5mm x 6mm)
RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

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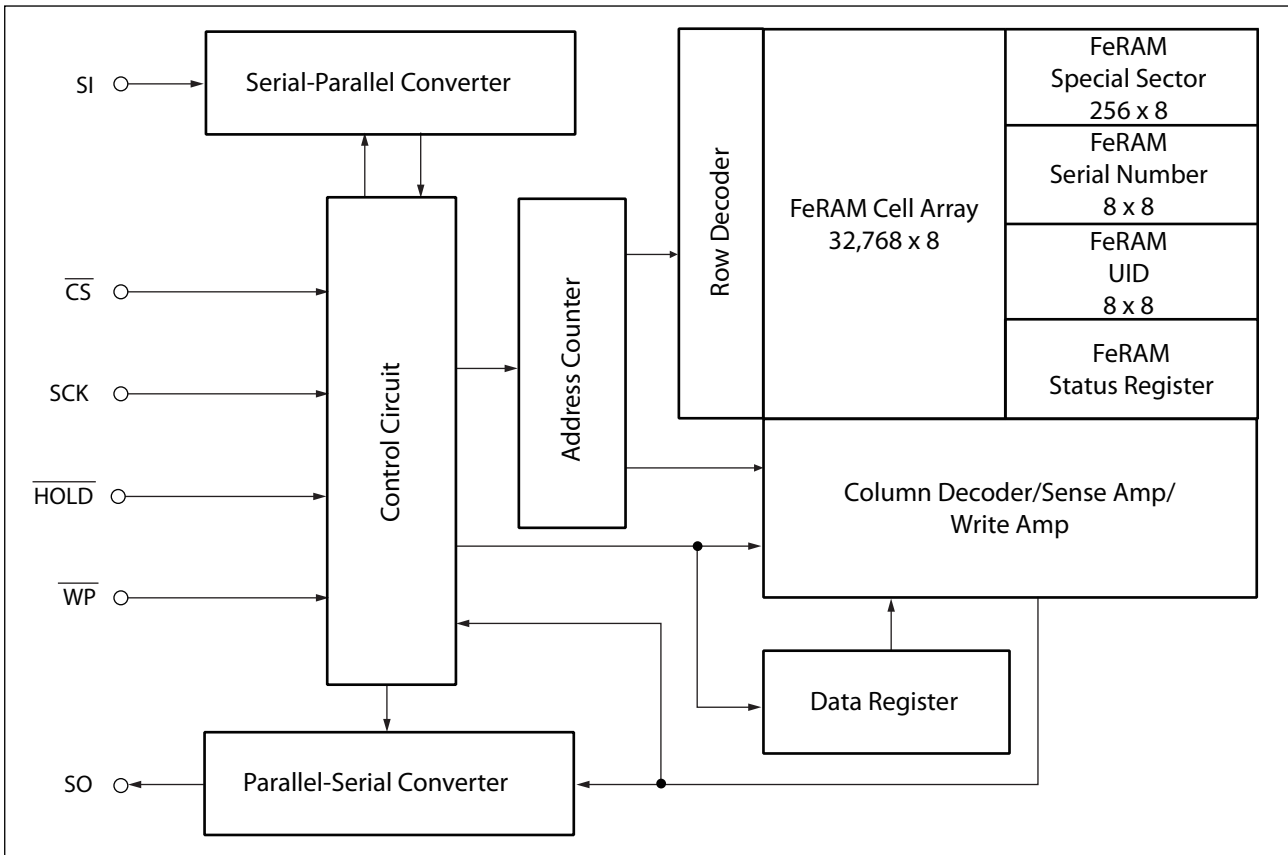
■ PIN ASSIGNMENT



■ PIN FUNCTIONAL DESCRIPTIONS

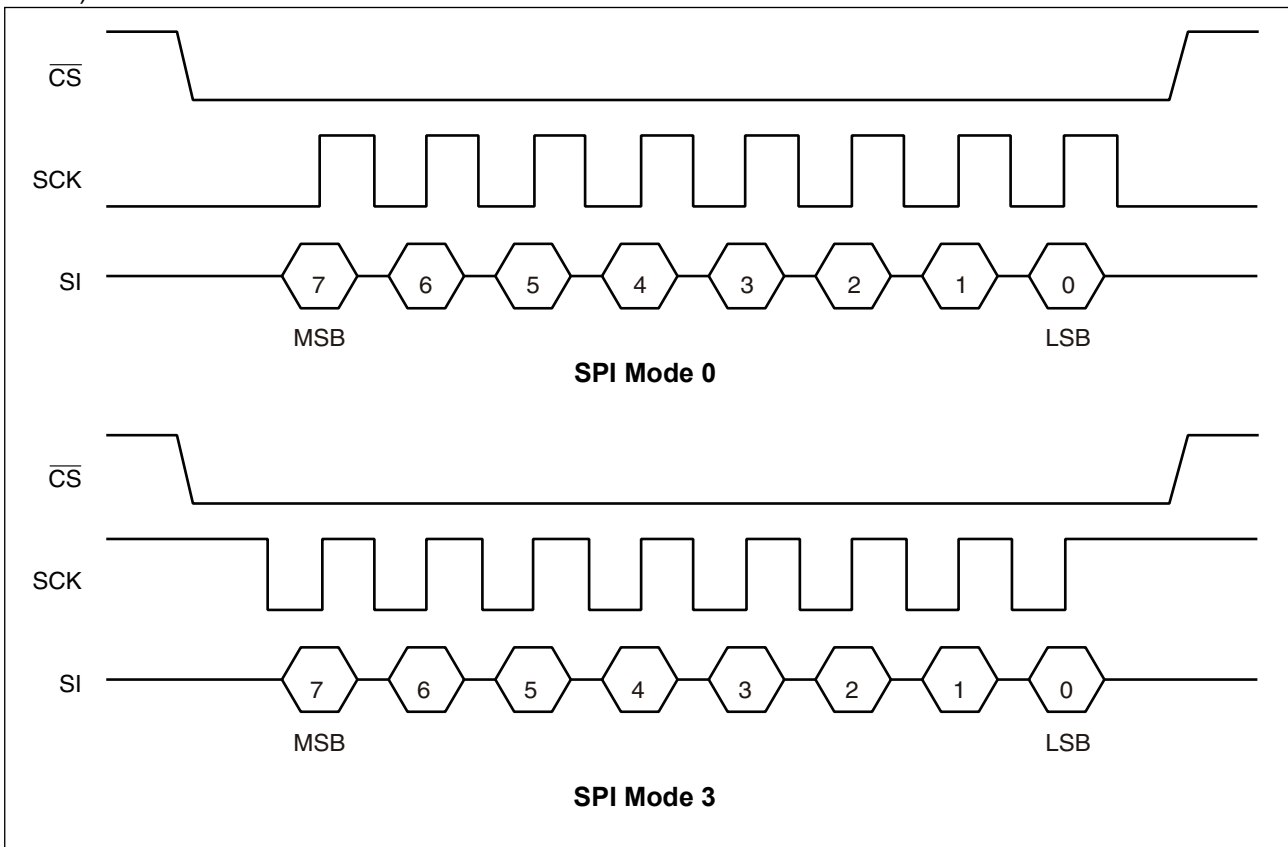
| Pin No. | Pin Name | Functional description |
|---------|-------------------|--|
| 1 | \overline{CS} | Chip Select pin This is an input pin to make chips select. When \overline{CS} is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When \overline{CS} is "L" level, device is in select (active) status. \overline{CS} has to be "L" level before inputting op-code. |
| 3 | \overline{WP} | Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with \overline{WP} and WPEN. See "■ WRITING PROTECT" for detail. |
| 7 | \overline{HOLD} | Hold pin This pin is used to interrupt serial input/output without making chips deselect. When \overline{HOLD} is "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. See "■ HOLD OPERATION" for detail. The Hold pin is pulled up internally to the VDD pin. |
| 6 | SCK | Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge. |
| 5 | SI | Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data. |
| 2 | SO | Serial Data Output pin This is an output pin of serial data. Reading data of FeRAM memory cell array and status register data are output. This is High-Z during standby. |
| 8 | VDD | Supply Voltage pin |
| 4 | VSS | Ground pin |

■ BLOCK DIAGRAM



■ SPI MODE

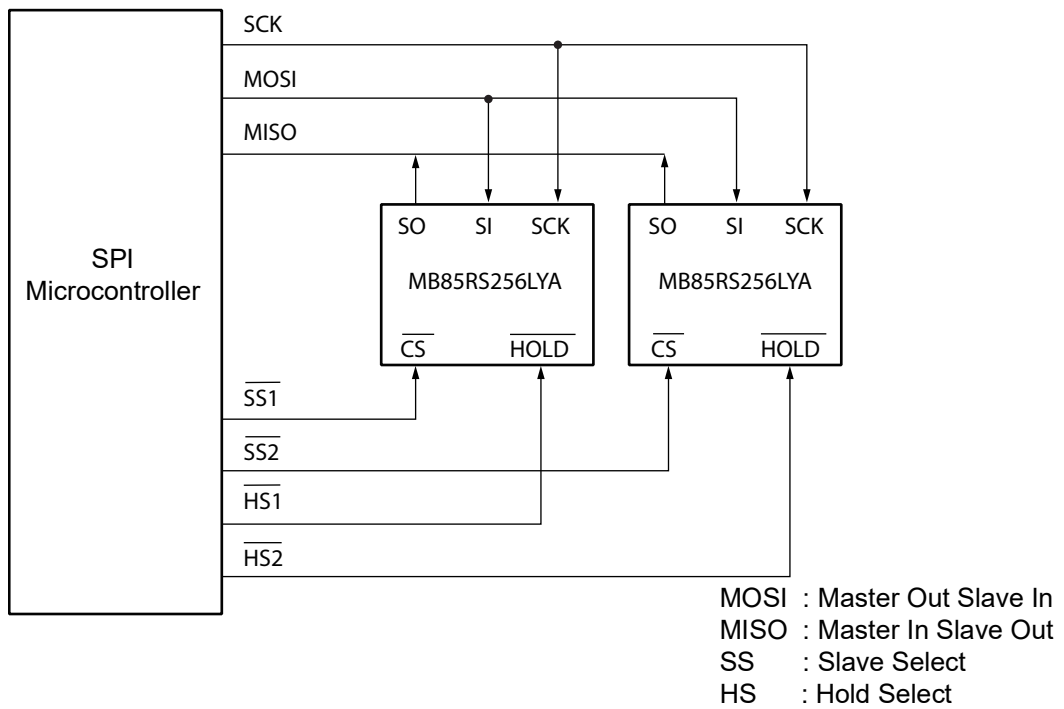
MB85RS256LYA corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0), and SPI mode 3 (CPOL = 1, CPHA = 1).



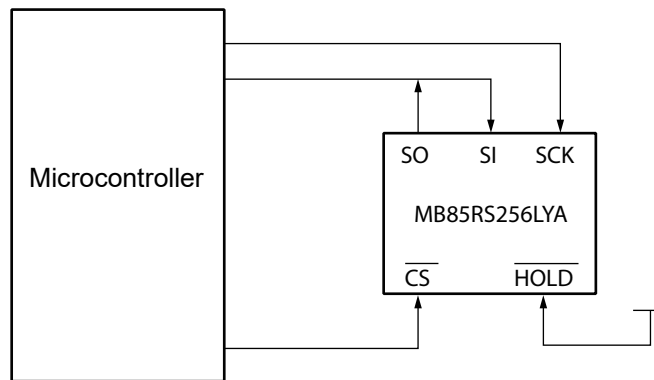
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■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS256LYA works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



System Configuration with SPI Port



System Configuration without SPI Port

■ STATUS REGISTER

| Bit No. | Bit Name | Function |
|---------|----------|--|
| 7 | WPEN | <p>Status Register Write Protect</p> <p>This is a bit composed of nonvolatile memories (FeRAM). WPEN protects writing to a status register (refer to “■ WRITING PROTECT”) relating with \overline{WP} input. Writing with the WRSR command and reading with the RDSR command are possible.</p> |
| 6 to 4 | — | <p>Not Used Bits</p> <p>These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.</p> |
| 3 | BP1 | <p>Block Protect</p> <p>This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to “■ BLOCK PROTECT”). Writing with the WRSR command and reading with the RDSR command are possible.</p> |
| 2 | BP0 | |
| 1 | WEL | <p>Write Enable Latch</p> <p>This indicates FeRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations.</p> <ul style="list-style-type: none"> After power ON. After WRDI command recognition. <p>Achieving continuous writing mode, WEL is not reset after following operations making it possible to execute writing commands continuously.</p> <ul style="list-style-type: none"> After WRSR command recognition. After WRITE command recognition. After WRSN command recognition. After SSWR command recognition. |
| 0 | 0 | This is a bit fixed to “0”. |

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■ OP-CODE

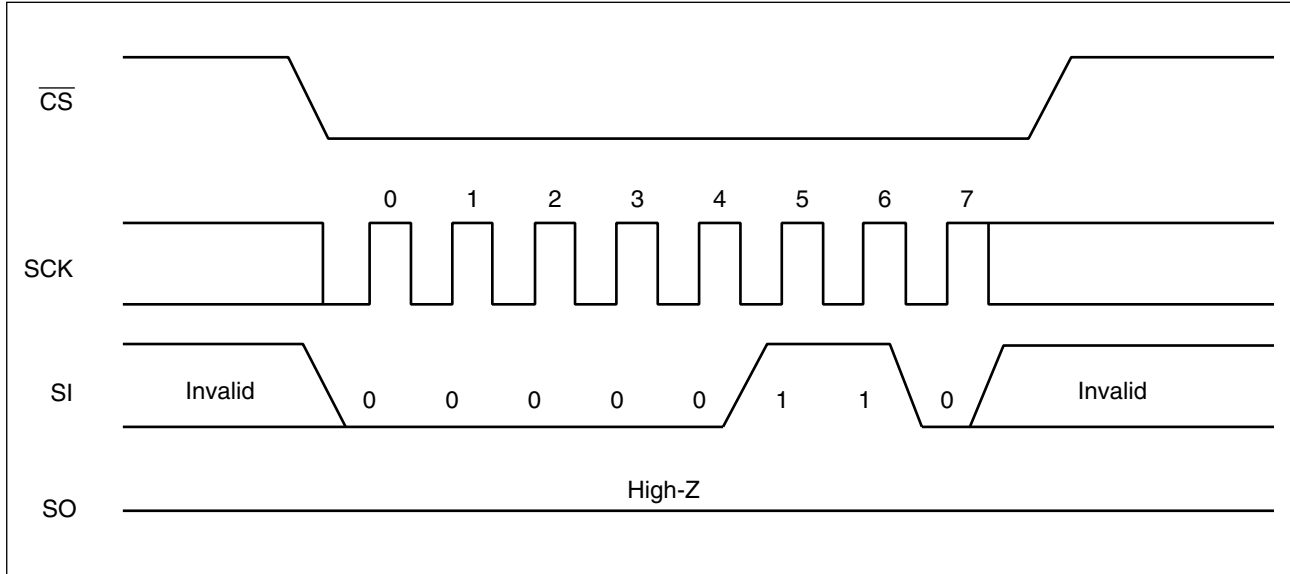
MB85RS256LYA accepts 14 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If \overline{CS} is risen while inputting op-code, the command are not performed.

| Name | Description | Op-code |
|-------|--------------------------|------------------------|
| WREN | Set Write Enable Latch | 0000 0110 _B |
| WRDI | Reset Write Enable Latch | 0000 0100 _B |
| RDSR | Read Status Register | 0000 0101 _B |
| WRSR | Write Status Register | 0000 0001 _B |
| READ | Read Memory Code | 0000 0011 _B |
| WRITE | Write Memory Code | 0000 0010 _B |
| FSTRD | Fast Read Memory Code | 0000 1011 _B |
| RDID | Read Device ID | 1001 1111 _B |
| RUID | Read Unique ID | 0100 1100 _B |
| WRSN | Write Serial Number | 1100 0010 _B |
| RDSN | Read Serial Number | 1100 0011 _B |
| SSWR | Write Special Sector | 0100 0010 _B |
| SSRD | Read Special Sector | 0100 1011 _B |
| FSSRD | Fast Read Special Sector | 0100 1001 _B |
| RFU | Reserved | 1100 1110 _B |
| | | 1100 1111 _B |
| | | 1100 1100 _B |

■ COMMAND

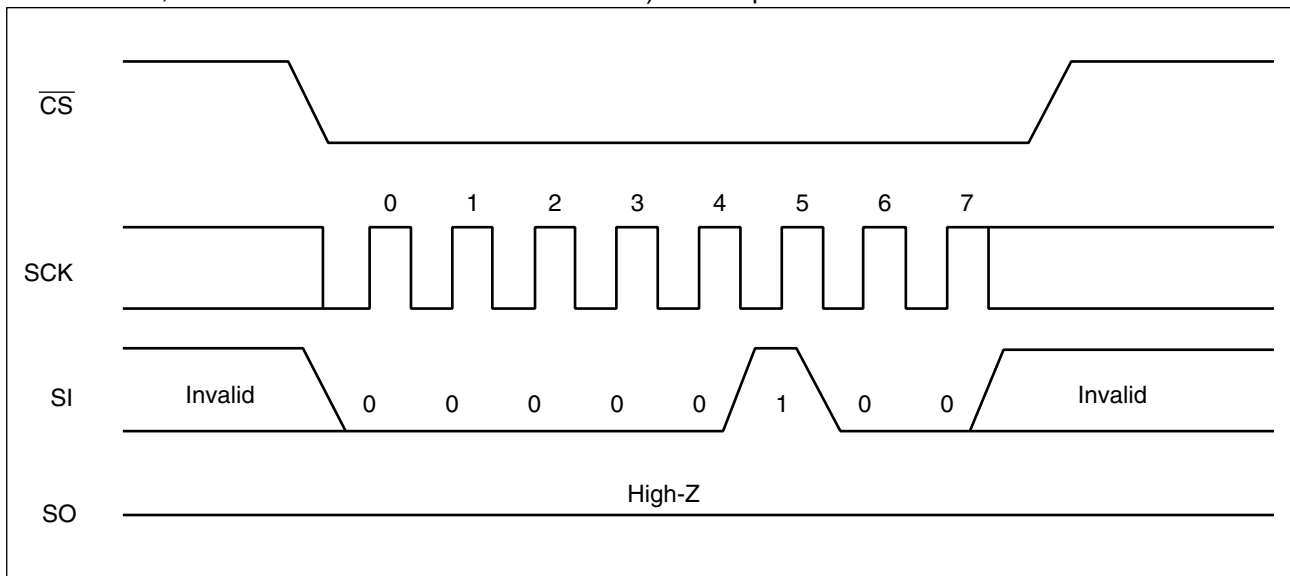
• WREN

The WREN command sets WEL (Write Enable Latch) bit to 1. WEL has to be set with the WREN command before writing operation (WRSR command, WRITE command, WRSN command and SSWR command) .



• WRDI

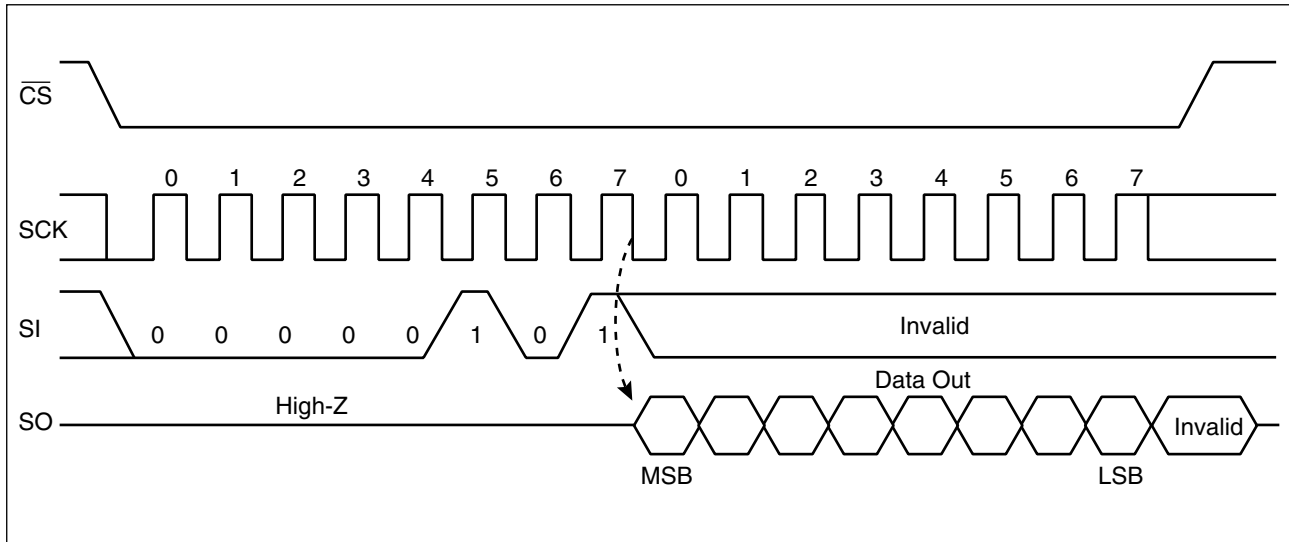
The WRDI command resets WEL (Write Enable Latch) bit to 0. Writing operation (WRSR command, WRITE command, WRSN command and SSWR command) are not performed when WEL is reset.



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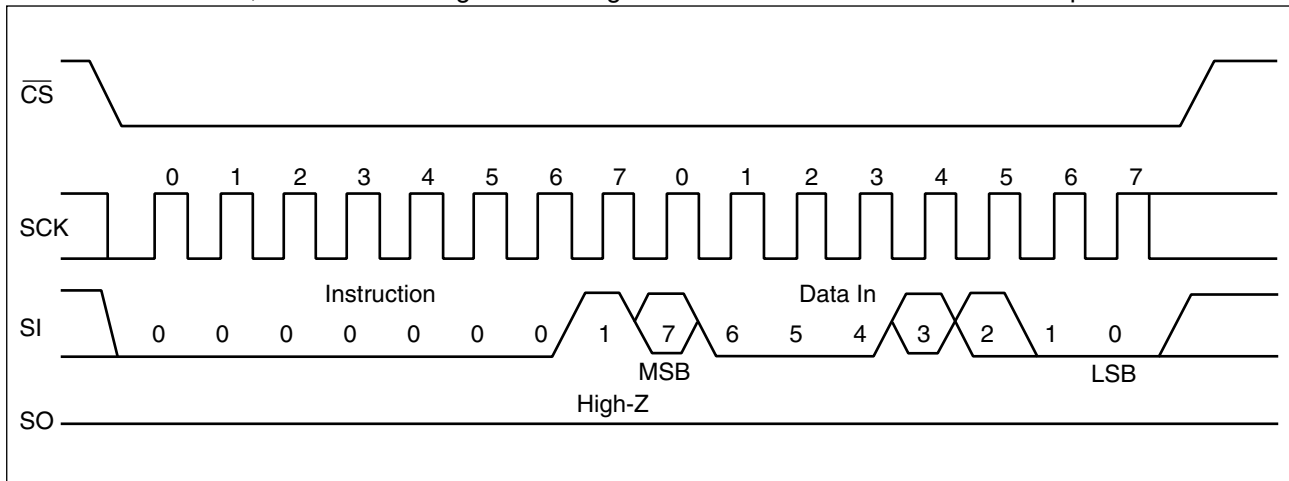
• RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of \overline{CS} .



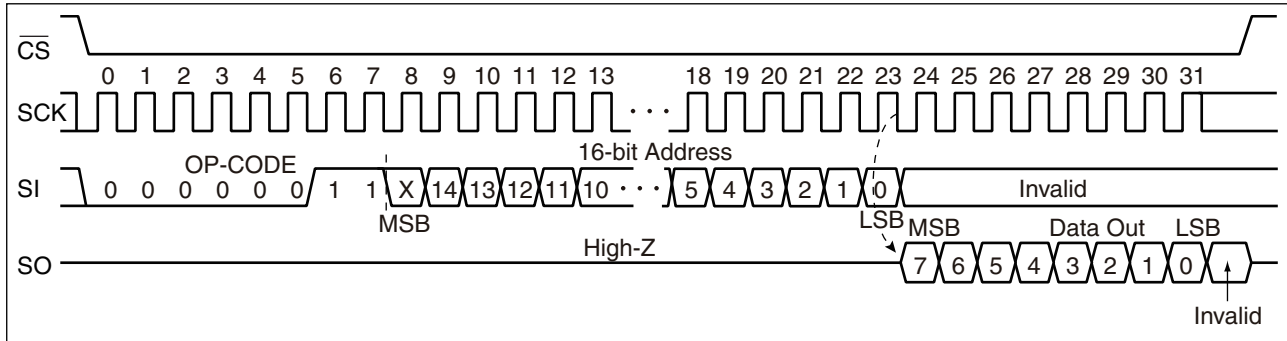
• WRSR

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored. \overline{WP} signal level shall be fixed before performing WRSR command, and do not change the \overline{WP} signal level until the end of command sequence.



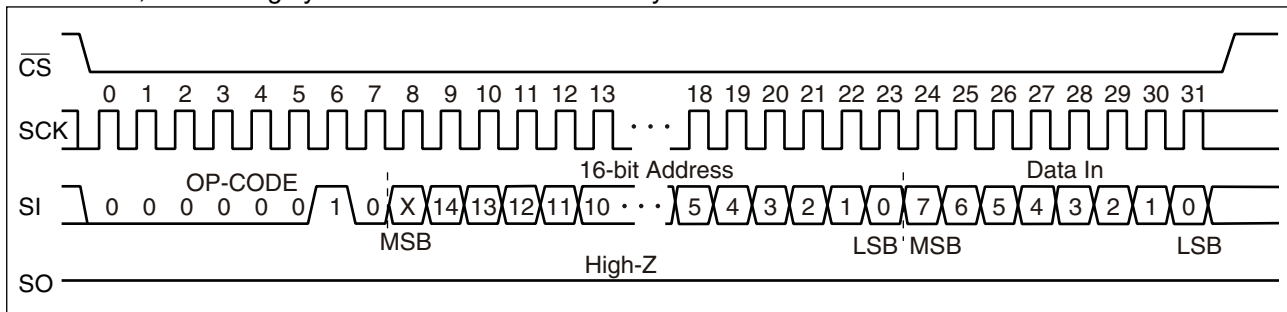
• READ

The READ command reads FeRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The most significant address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



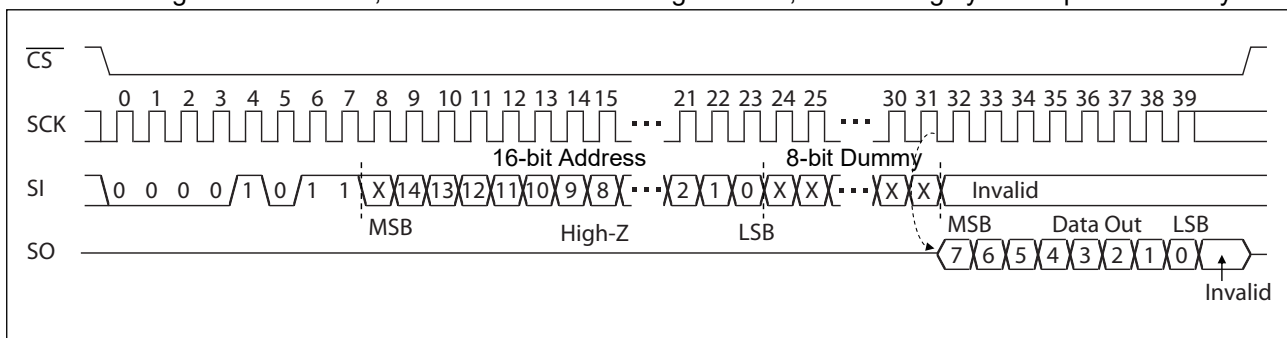
• WRITE

The WRITE command writes data to FeRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The most significant address bit is invalid. When 8 bits of writing data is input, data is written to FeRAM memory cell array. Risen \overline{CS} will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before \overline{CS} rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely.



• FSTRD

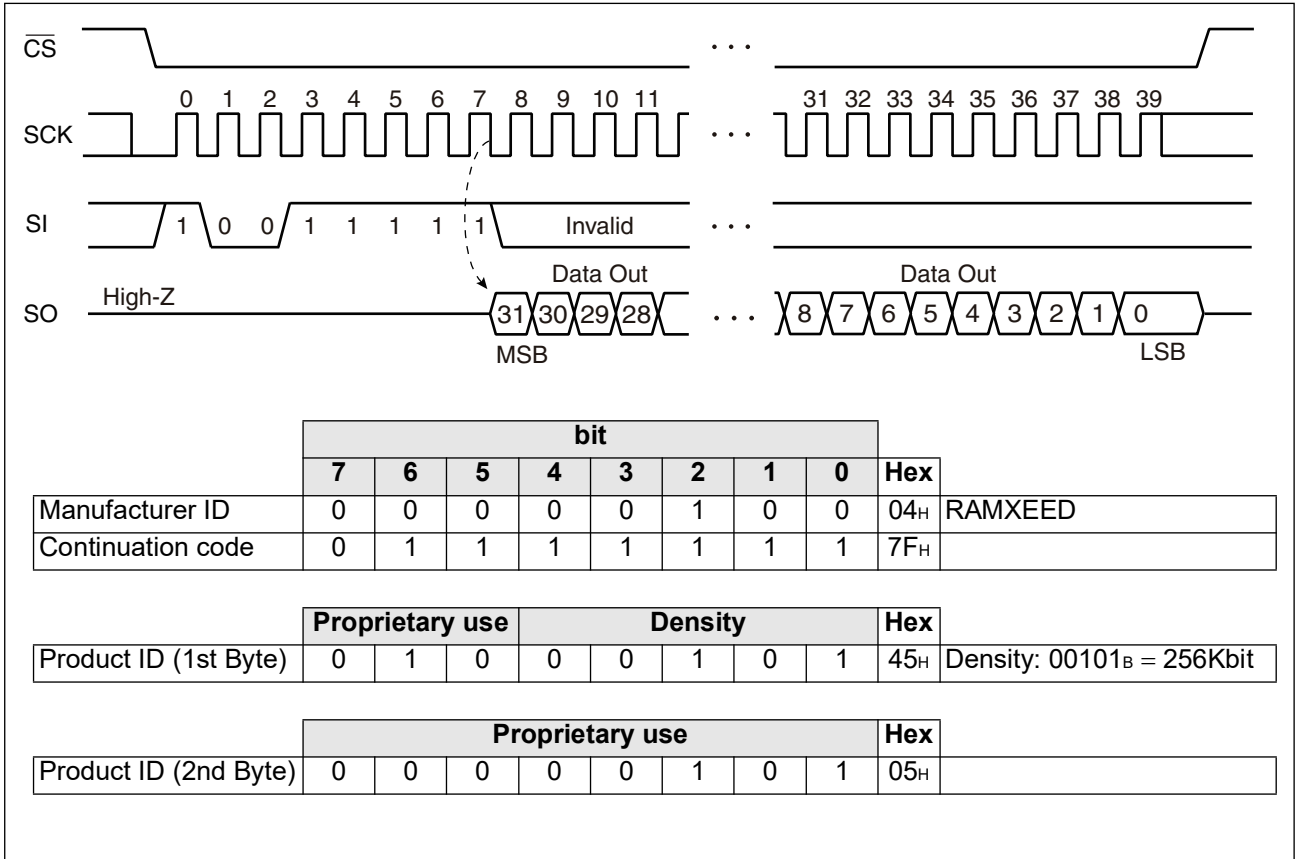
The FSTRD command reads FeRAM memory cell array data. Arbitrary 16bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 1-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the FSTRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



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• RDID

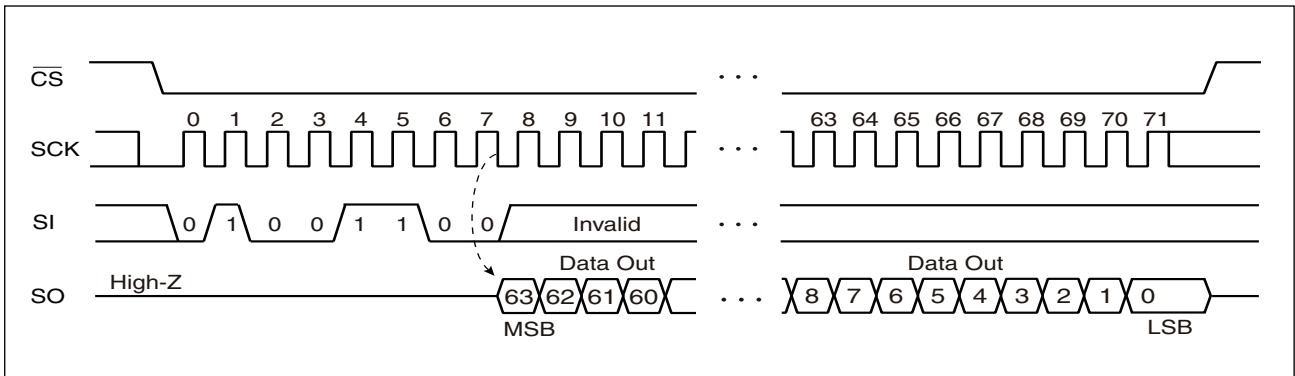
The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, 32-bit Device ID is output by continuously sending SCK clock, and SO holds the output state of the last bit until CS is risen.



• RUID

The RUID command reads an unique ID which is defined in 64bits for each device. After performing RUID op-code to SI, 64-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK.

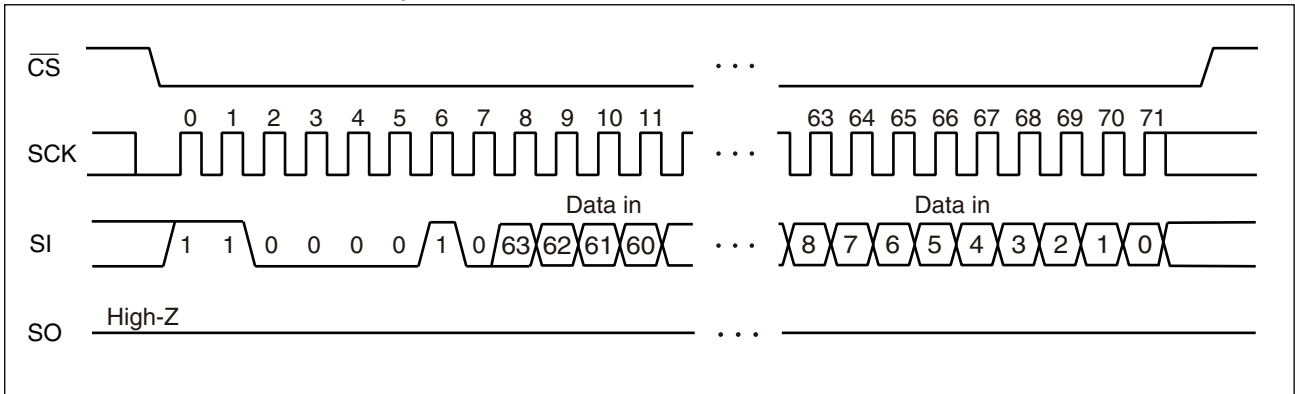
The unique ID is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



•WRSN

The WRSN command writes data to serial number region which is allowed to write only one time. After performing WRSN op-code to SI, 64bits of writing data is input. Once wrote, the serial number region is protected, disabling to overwrite even when issuing WRSN command.

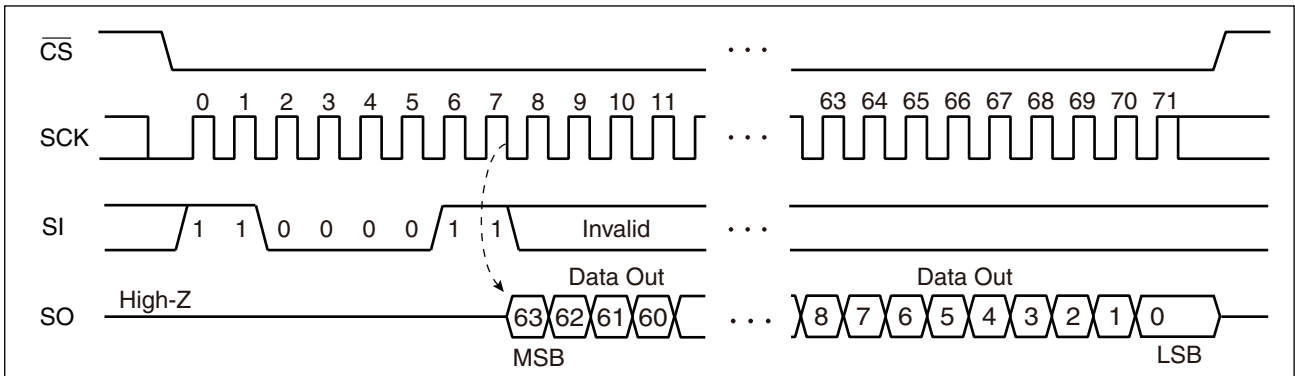
\overline{WP} signal level shall be fixed before performing WRSN command, and do not change the \overline{WP} signal level until the end of command sequence.



•RDSN

The RDSN command reads 64 bits of serial number which is written using WRSN command. After performing RDSN op-code to SI, 64-cycle clock to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. When reading serial number from devices which no WRSN command is executed, "0" for all bits are output.

The serial number is stable between before and after reflow. Refer "■ REFLOW CONDITIONS AND FLOOR LIFE" for the reflow condition.

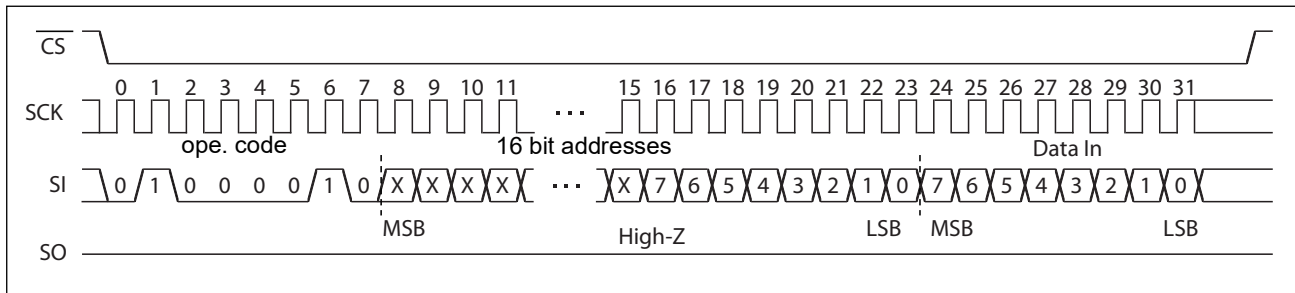


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- SSWR

The SSWR command writes data to special sector (a special region of 256 Byte in FeRAM). SSWR op-code, arbitrary 16 bits address and 8-bit writing data are input to SI. The 8-bit upper address is invalid. When input of 8-bit writing data is completed, it starts writing data to special sector. Risen \overline{CS} will terminate the SSWR command, but if you continue the writing data for each before \overline{CS} rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, roll over is not happen, the data hereafter is ignored.

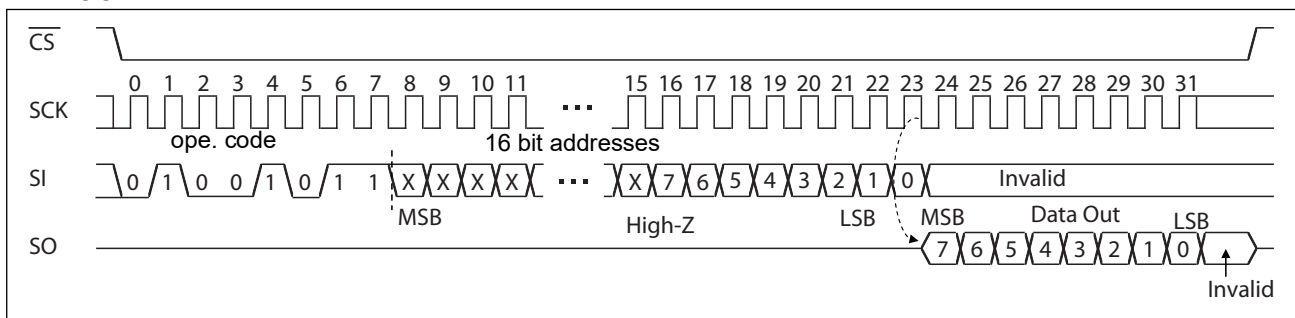
The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



- SSRD

The SSRD command reads data from special sector (a special region of 256 Byte in FeRAM). SSWR op-code and arbitrary 16 bits address are input to SI. The 8-bit upper address is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the SSRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, roll over is not happen.

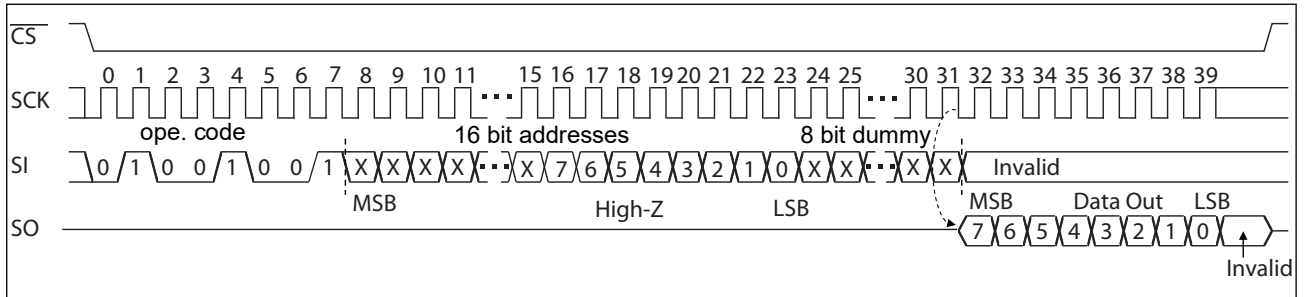
The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



- FSSRD

The SSRD command reads data from special sector (a special region of 256 Byte in FeRAM). SSWR op-code and arbitrary 16 bits address are input to SI followed by 8 bits dummy. The 8-bit upper address is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the SSRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, roll over is not happen.

The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.



■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

| BP1 | BP0 | Protected Block |
|-----|-----|--|
| 0 | 0 | None |
| 0 | 1 | 6000 _H to 7FFF _H (upper 1/4) |
| 1 | 0 | 4000 _H to 7FFF _H (upper 1/2) |
| 1 | 1 | 0000 _H to 7FFF _H (all) |

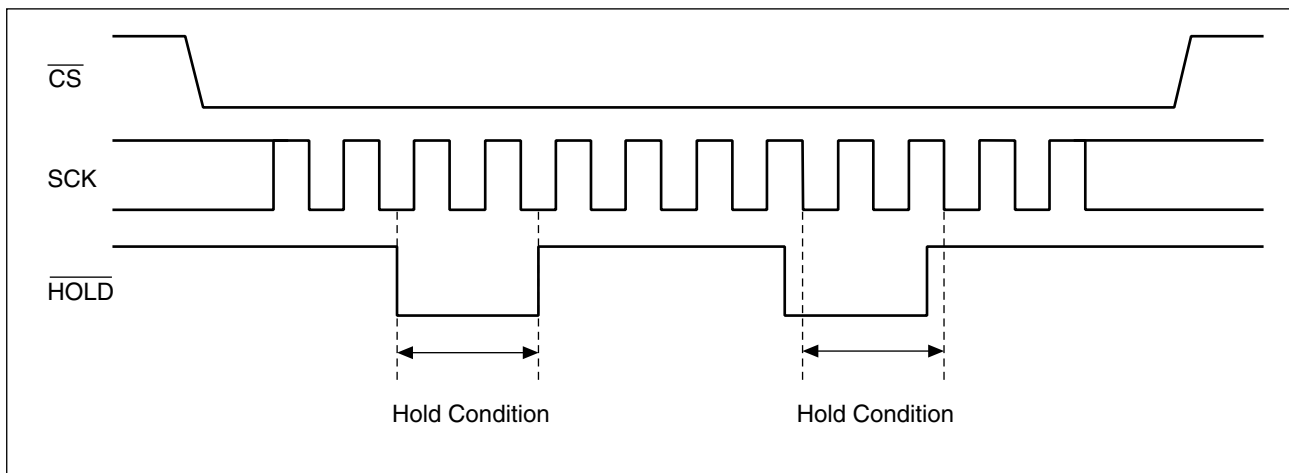
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, WP as shown in the table.

| WEL | WPEN | WP | Protected Blocks | Unprotected Blocks | Status Register |
|-----|------|----|------------------|--------------------|-----------------|
| 0 | X | X | Protected | Protected | Protected |
| 1 | 0 | X | Protected | Unprotected | Unprotected |
| 1 | 1 | 0 | Protected | Unprotected | Protected |
| 1 | 1 | 1 | Protected | Unprotected | Unprotected |

■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{\text{HOLD}}$ is "L" level while $\overline{\text{CS}}$ is "L" level. The timing for starting and ending hold status depends on the SCK to be "H" level or "L" level when a HOLD pin input is transitioned to the hold condition as shown in the diagram below. In case the HOLD pin transitioned to "L" level when SCK is "L" level, return the HOLD pin to "H" level at SCK being "L" level. In the same manner, in case the HOLD pin transitioned to "L" level when SCK is "H" level, return the HOLD pin to "H" level at SCK being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If $\overline{\text{CS}}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|-------------------------------|-----------|--------|----------------|------|
| | | Min | Max | |
| Power supply voltage* | V_{DD} | - 0.5 | + 2.5 | V |
| Input voltage* | V_{IN} | - 0.5 | $V_{DD} + 0.5$ | V |
| Output voltage* | V_{OUT} | - 0.5 | $V_{DD} + 0.5$ | V |
| Operation ambient temperature | T_A | - 40 | + 125 | °C |
| Storage temperature | T_{stg} | - 55 | + 150 | °C |

*: These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|---|----------|-------|------|-------|------|
| | | Min | Typ | Max | |
| Power supply voltage* ¹ | V_{DD} | 1.70 | 1.80 | 1.95 | V |
| Operation ambient temperature* ² | T_A | - 40 | — | + 125 | °C |

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

MB85RS256LYA

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

| Parameter | Symbol | Condition | Value | | | Unit | |
|----------------------------------|-----------------|---|-----------------------|--------------------------------|-----------------------|------|----|
| | | | Min | Typ (T _A =25 °C) | Max | | |
| Input leakage current*1 | I _{LI} | $\overline{CS} = V_{DD}$ | 25 °C | — | — | 1 | μA |
| | | | 125 °C | — | — | 2 | |
| | | $\overline{WP}, \overline{SCK}, \overline{CS}$ SI = 0 V to V _{DD} | 25 °C | — | — | 1 | |
| | | | 125 °C | — | — | 2 | |
| | | HOLD = 0 V to V _{DD} | 25 °C | — | — | 100 | |
| | | | 125 °C | — | — | 100 | |
| Output leakage current*2 | I _{LO} | SO = 0 V to V _{DD} | 25 °C | — | — | 1 | μA |
| | | | 125 °C | — | — | 2 | |
| Operating power supply current*3 | I _{DD} | SCK = 50MHz | — | 2.38 | 3.0 | mA | |
| Standby current | I _{SB} | SCK = SI = \overline{CS} = $\overline{WP} = V_{DD}$ | — | 5.0 | 150 | μA | |
| Input high voltage | V _{IH} | V _{DD} = 1.7 V to 1.95 V | V _{DD} × 0.8 | — | V _{DD} + 0.5 | V | |
| Input low voltage | V _{IL} | V _{DD} = 1.7 V to 1.95 V | - 0.5 | — | V _{DD} × 0.2 | V | |
| Output high voltage | V _{OH} | I _{OH} = - 2 mA | V _{DD} - 0.5 | — | — | V | |
| Output low voltage | V _{OL} | I _{OL} = 2 mA | — | — | 0.4 | V | |
| Pull up resistance for HOLD | R _P | — | 36 | 66 | 230 | kΩ | |

*1 : Applicable pin : \overline{CS} , \overline{WP} , SCK, SI

*2 : Applicable pin : SO

*3 : Input voltage magnitude : V_{DD} - 0.2 V or V_{SS}

2. AC Characteristics

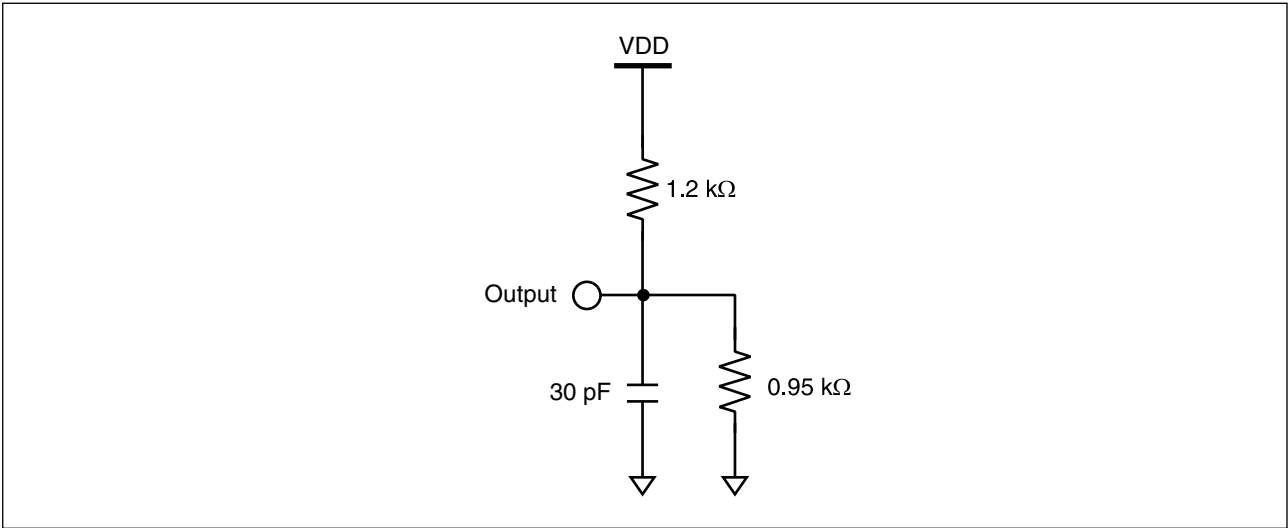
| Parameter | Symbol | Value | | Unit | Condition V _{DD} |
|---------------------------|------------------|-------|-----|------|-----------------------------------|
| | | Min | Max | | |
| SCK clock frequency | f _{CK} | — | 50 | MHz | all commands except for READ/SSRD |
| | | — | 40 | | READ command |
| | | — | 10 | | SSRD command |
| Clock high time | t _{CH} | 9 | — | ns | |
| Clock low time | t _{CL} | 9 | — | ns | |
| Chip select set up time | t _{CSU} | 5 | — | ns | |
| Chip select hold time | t _{CSH} | 5 | — | ns | |
| Output disable time | t _{OD} | — | 10 | ns | |
| Output data valid time | t _{ODV} | — | 9 | ns | *1 |
| Output hold time | t _{OH} | 0 | — | ns | |
| Deselect time | t _D | 40 | — | ns | |
| Data in rising time | t _R | — | 50 | ns | |
| Data falling time | t _F | — | 50 | ns | |
| Data set up time | t _{SU} | 5 | — | ns | |
| Data hold time | t _H | 5 | — | ns | |
| HOLD set uptime | t _{HS} | 10 | — | ns | — |
| HOLD hold time | t _{HH} | 10 | — | ns | — |
| HOLD output floating time | t _{HZ} | — | 20 | ns | — |
| HOLD output active time | t _{LZ} | — | 20 | ns | — |

*1: In SSRD command, 60ns(max.)

AC Test Condition

| | |
|-------------------------------|---|
| Power supply voltage | : 1.7 V to 1.95 V Operation |
| Operation ambient temperature | : -40 °C to +125 °C |
| Input voltage magnitude | : $V_{DD} \times 0.8 \leq V_{IH} \leq V_{DD}$ $0 \leq V_{IL} \leq V_{DD} \times 0.2$ |
| Input rising time | : 5 ns |
| Input falling time | : 5 ns |
| Input judge level | : $V_{DD}/2$ |
| Output judge level | : $V_{DD}/2$ |

AC Load Equivalent Circuit

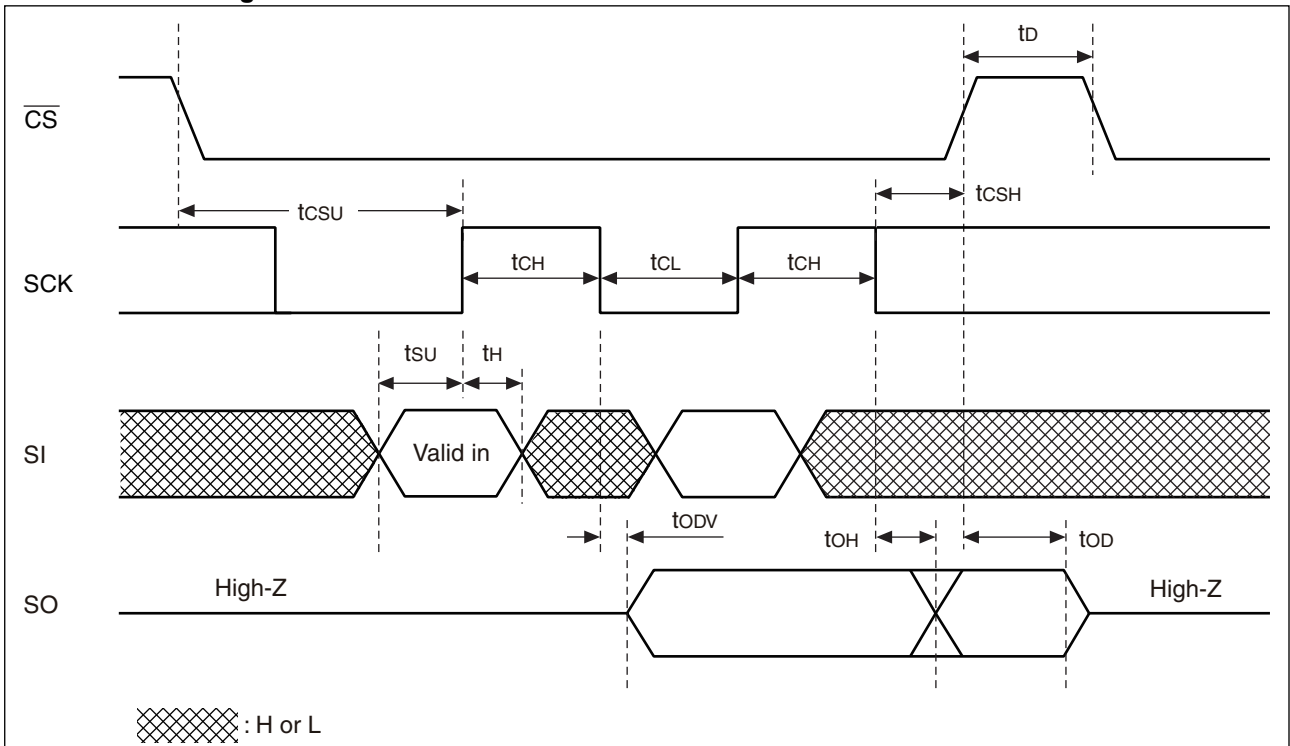


3. Pin Capacitance

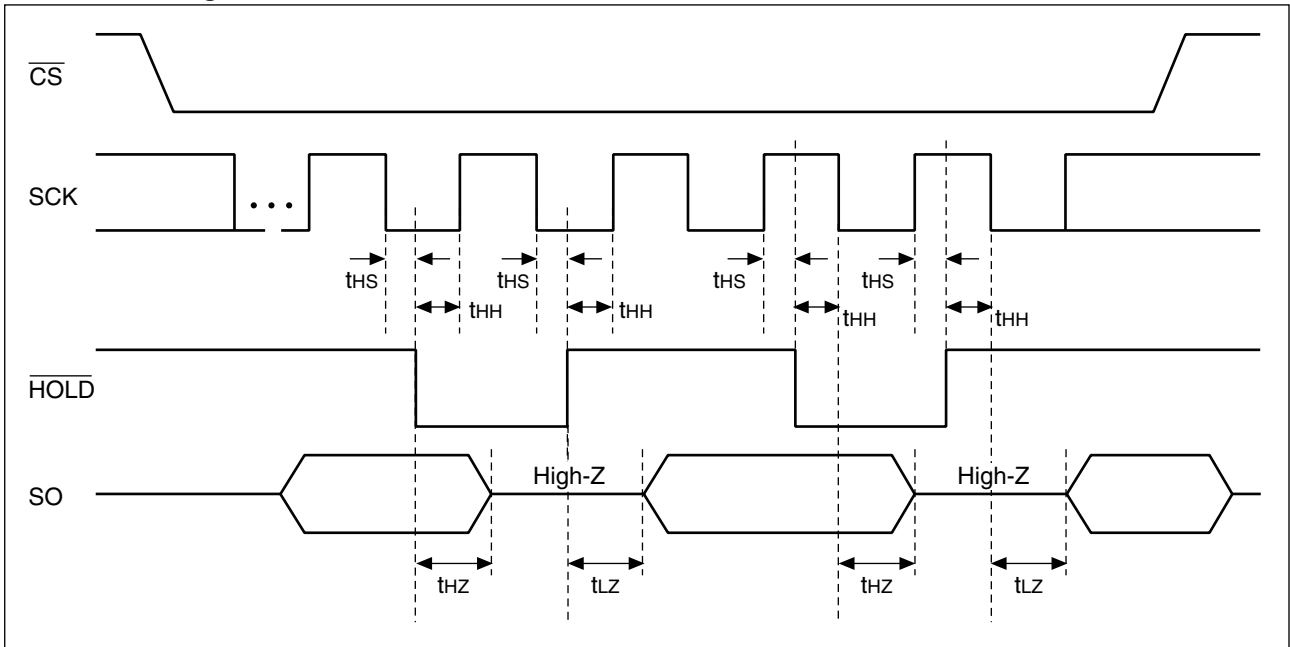
| Parameter | Symbol | Condition | Value | | Unit |
|--------------------|--------|---|-------|-----|------|
| | | | Min | Max | |
| Output capacitance | C_O | $V_{DD} = 1.8 \text{ V}$, $V_{IN} = V_{OUT} = 0 \text{ V to } V_{DD}$, $f = 1 \text{ MHz}$, $T_A = +25 \text{ }^\circ\text{C}$ | — | 8 | pF |
| Input capacitance | C_I | | — | 6 | pF |

■ TIMING DIAGRAM

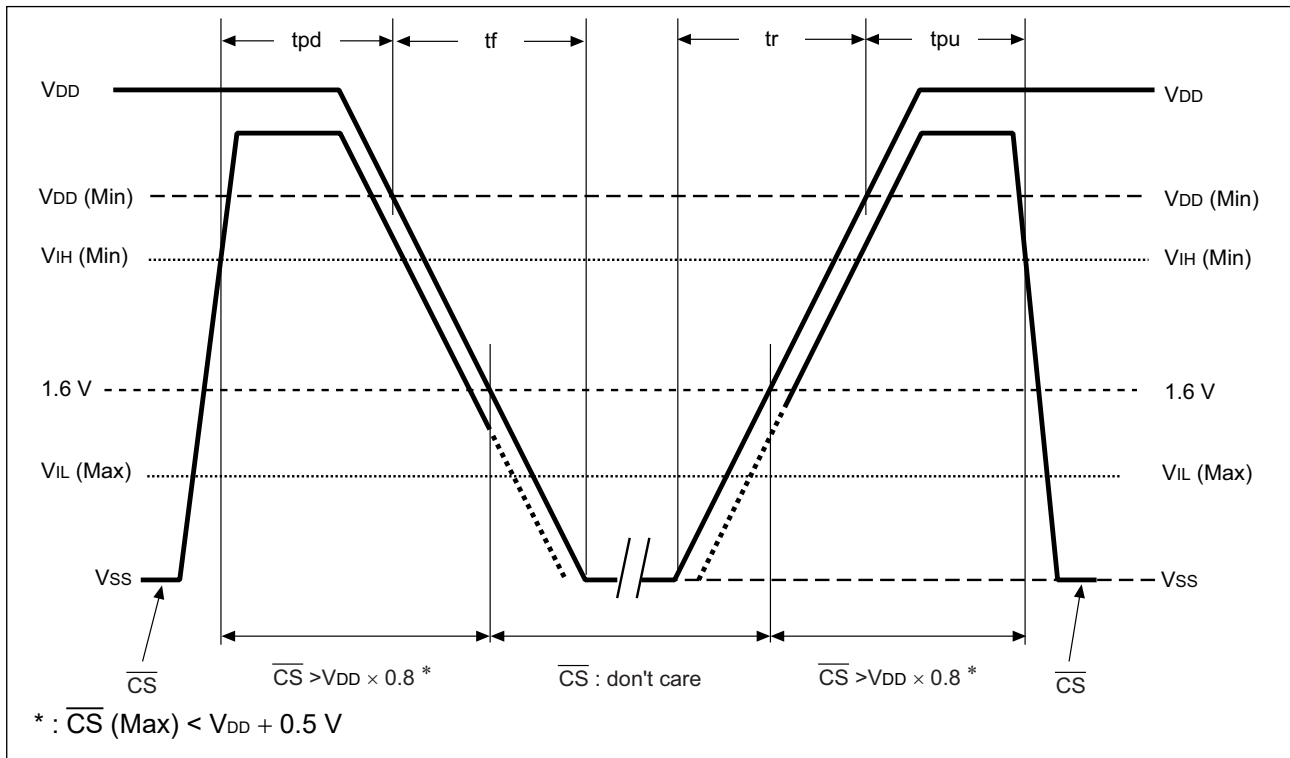
• Serial Data Timing



• Hold Timing



■ POWER ON/OFF SEQUENCE



In case relative short V_{DD} pulse whose peak level is beyond 1.6 is applied, please set V_{DD} falling time, t_f , longer than 0.4ms/V. (When V_{DD} rises beyond 1.6V, and falls just after, if this term is very short the device may loose its function.).

| Parameter | Symbol | Value | | Unit |
|--|--------|-------|-----|---------------|
| | | Min | Max | |
| \overline{CS} level hold time at power OFF | tpd | 400 | — | ns |
| \overline{CS} level hold time at power ON | tpu | 450 | — | μs |
| Power supply rising time | tr | 0.05 | — | ms/V |
| Power supply falling time | tf | 0.1 | — | ms/V |

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

| Parameter | Value | | Unit | Remarks |
|------------------------|------------------|-----|-------|---|
| | Min | Max | | |
| Read/Write Endurance*1 | 10 ¹³ | — | Times | Operation Ambient Temperature T _A = + 125 °C |
| | 10 ¹⁴ | — | | Operation Ambient Temperature T _A = + 85 °C |
| Data Retention*2 | 10.1 or more*3 | — | Years | Operation Ambient Temperature T _A = + 125 °C |
| | 40.7 | — | | Operation Ambient Temperature T _A = + 105 °C |
| | 193.9 | — | | Operation Ambient Temperature T _A = + 85 °C |

*1: For details on the Read/Write endurance value, please refer to “■Read/Write endurance about FeRAM”.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

*3: Under evaluation for more than 10.1 years(+125 °C).

■ NOTE ON USE

We recommend programming of the device after reflow except for special sector region and serial number region. Data written before reflow cannot be guaranteed.

■ Read/Write endurance about FeRAM

The value for Read/Write endurance apply to the total number of read and write operations per row in FeRAM. This is because FeRAM needs writing operation after each reading operations. Each row in the memory array has 32 internal outputs, and 8 outputs are selected by A0 and A1. In continuous Read/Write operations, after selecting a certain address and automatically incrementing until A0 and A1 change from (0,0) to (1,1), the Read/Write count endurance count is totaled as one operation. Subsequently, when incrementing automatically and switching to the next row, each row is counted as a new Read/Write operation. If /CS is raised and then the same row is selected again, it is counted as the second operation for that row.

As an actual usage example, if you loop through and access only a memory area (64 bytes or 256 bytes) specified by a specific address in the entire memory area, the number of years it will take to reach 10¹⁴ times is as below.

As shown here, with a write endurance of 10¹⁴ times, even in extreme cases there is enough time before the upper limit is reached, and under normal conditions of use it can be used without worrying about the number of writes/reads.

| Operating frequency | Years reached when looping continuously through 64 byte area | Years reached when looping continuously through 256 byte area |
|---------------------|--|---|
| 50MHz | 34.1 | 131 |
| 40MHz | 42.6 | 164 |
| 20MHz | 85.1 | 328 |
| 10MHz | 170.0 | 657 |

MB85RS256LYA

■ ESD AND LATCH-UP

| Test | DUT | Value |
|--|--|-------------------------|
| ESD HBM (Human Body Model) JESD22-A114 compliant | MB85RS256LYAPNF-G-BCE1 MB85RS256LYAPNF-G-BCERE1 MB85RS256LYAPN-G-AWE1 MB85RS256LYAPN-G-AWEWE1 | $\geq 2000 \text{ V} $ |
| ESD CDM (Charged Device Model) JESD22-C101 compliant | | $\geq 1000 \text{ V} $ |
| Latch-Up (I-test) JESD78 compliant | | $\geq 125\text{mA} $ |
| Latch-Up (V_{supply} overvoltage test) JESD78 compliant | | $\geq 5.4\text{V}$ |

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ Current status on Contained Restricted Substances

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

■ ORDERING INFORMATION :

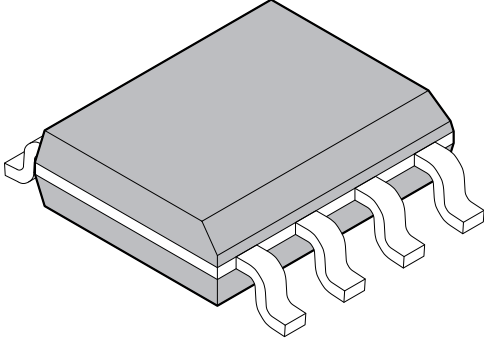
| Part number | Package | Shipping form | Minimum shipping quantity |
|--------------------------|----------------------------|-----------------------|---------------------------|
| MB85RS256LYAPNF-G-BCE1 | 8-pin plastic SOP (150mil) | Tube | — * |
| MB85RS256LYAPNF-G-BCERE1 | 8-pin plastic SOP (150mil) | Embossed Carrier tape | 1500 |
| MB85RS256LYAPN-G-AWE1 | 8-pin plastic DFN | Tray | — * |
| MB85RS256LYAPN-G-AWEWE1 | 8-pin plastic DFN | Embossed Carrier tape | 1500 |

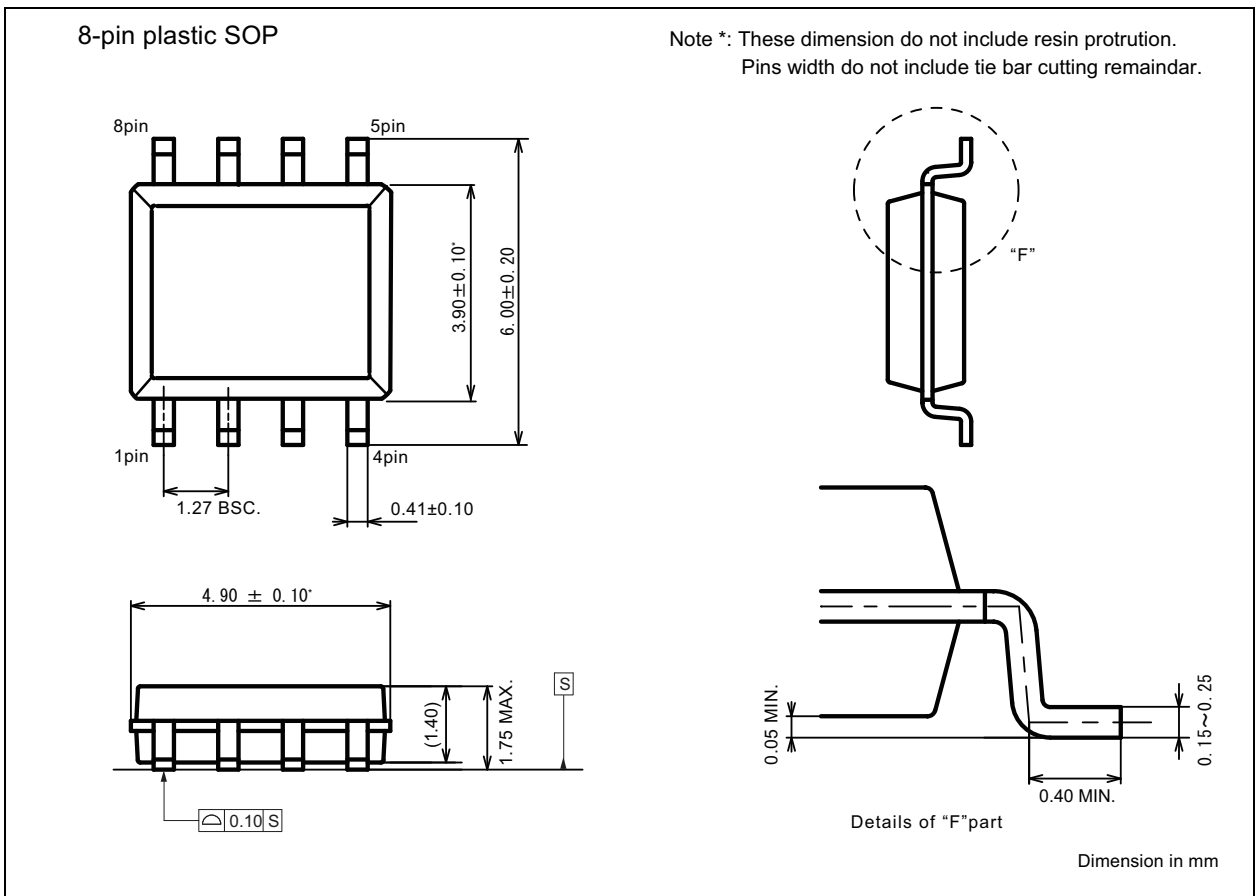
* : Please contact our sales office about minimum shipping quantity.

MB85RS256LYA

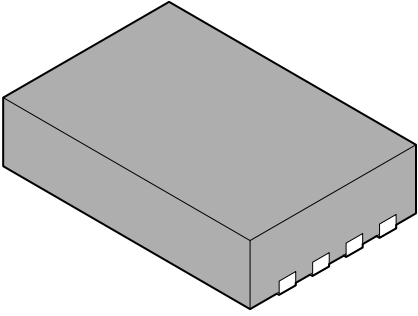
■ PACKAGE DIMENSION

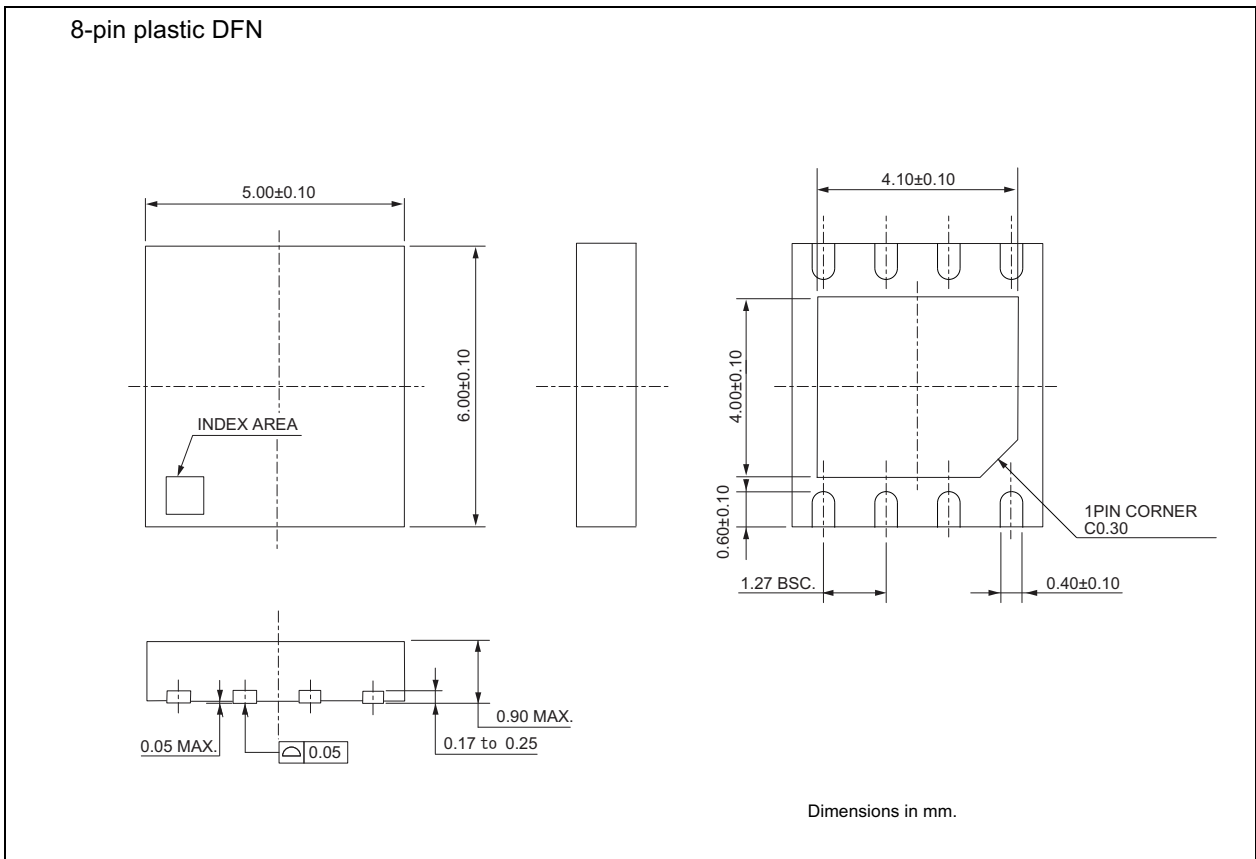
(1) MB85RS256LYAPNF-G-BCE1/MB85RS256LYAPNF-G-BCERE1

| | | |
|--|--------------------------------|-----------------|
| <p>8-pin plastic SOP(150mil)</p>  | Lead pitch | 1.27mm |
| | Package width x Package length | 3.90mm x 4.90mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.75mm MAX. |
| | | |



(2) MB85RS256LYAPN-G-AWE1/MB85RS256LYAPN-G-AWEWE1

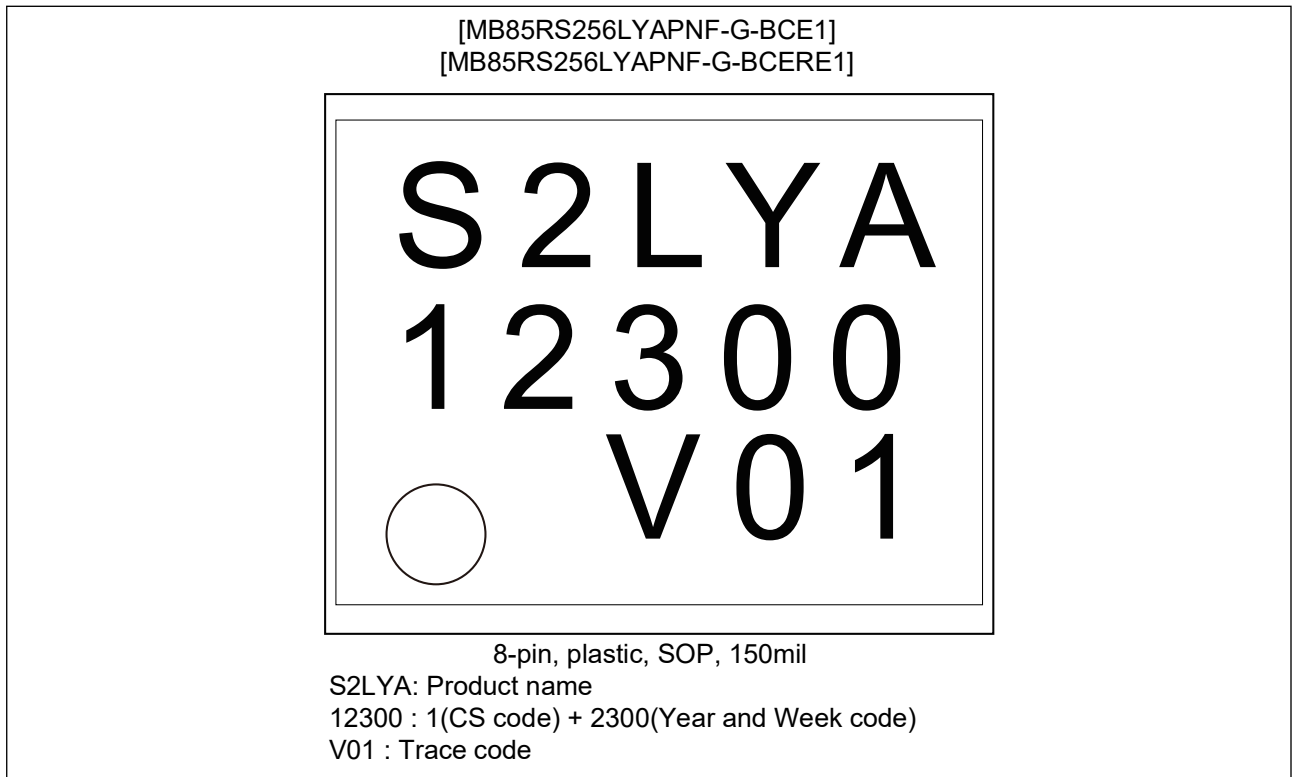
| | | |
|--|-----------------------------------|-------------------|
| <p>8-pin plastic DFN</p>  | Lead pitch | 1.27 mm |
| | Package width x Package length | 5.00 mm × 6.00 mm |
| | Sealing method | Plastic mold |
| | Mounting height | 0.90 mm MAX |
| | | |



MB85RS256LYA

■ MARKING (Example)

(1) MB85RS256LYAPNF-G-BCE1/MB85RS256LYAPNF-G-BCERE1



(2) MB85RS256LYAPN-G-AWE1/MB85RS256LYAPN-G-AWEWE1



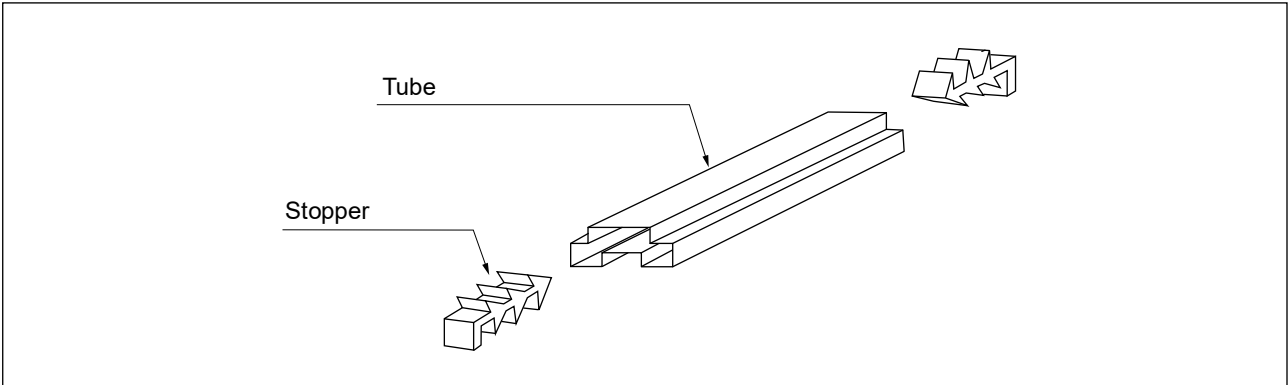
■ PACKING INFORMATION

(1) MB85RS256LYAPNF-G-BCE1/MB85RS256LYAPNF-G-BCERE1

1. Tube (MB85RS256LYAPNF-G-BCE1)

1.1 Tube Dimensions

- Tube/stopper shape (example)



- Tube cross-sections and Maximum quantity

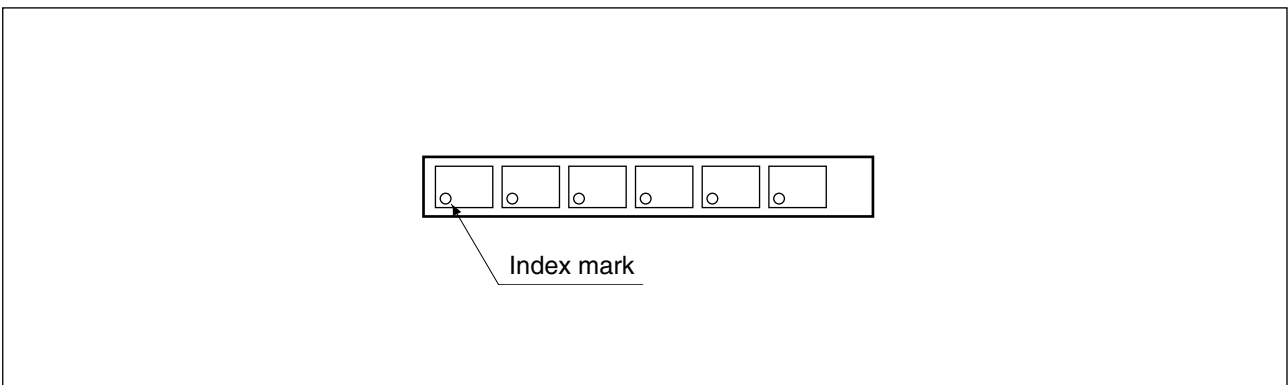
| Maximum quantity | | |
|------------------|---------------|---------------|
| pcs/tube | pcs/inner box | pcs/outer box |
| 85 | 4,250 | 17,000 |

tube length: 500

No heat resistance.
Package should not be baked by using tube.

(Dimensions in mm)

- Direction of index in tube



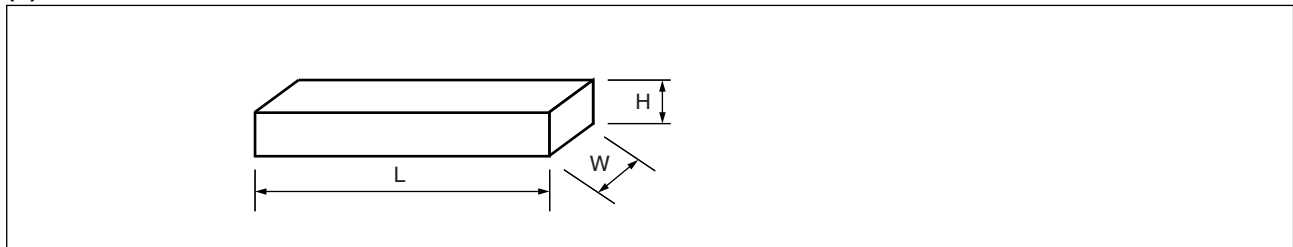
MB85RS256LYA

1.2 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

1.3 Dimensions for Containers

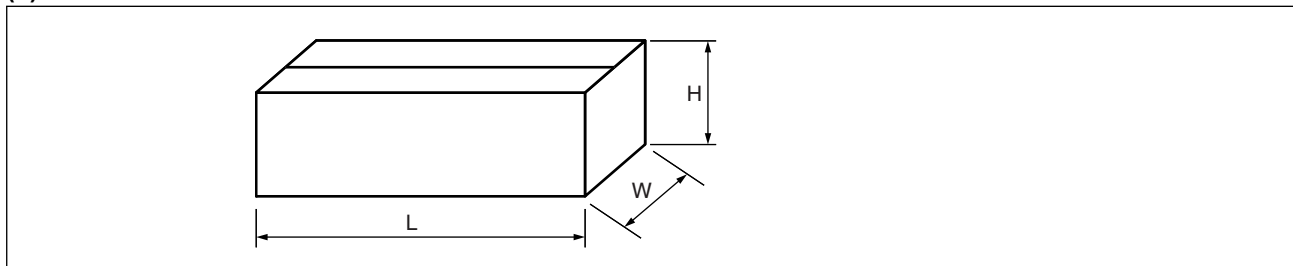
(1) Dimensions for inner box



| L | W | H |
|-----|-----|----|
| 540 | 125 | 75 |

(Dimensions in mm)

(2) Dimensions for outer box

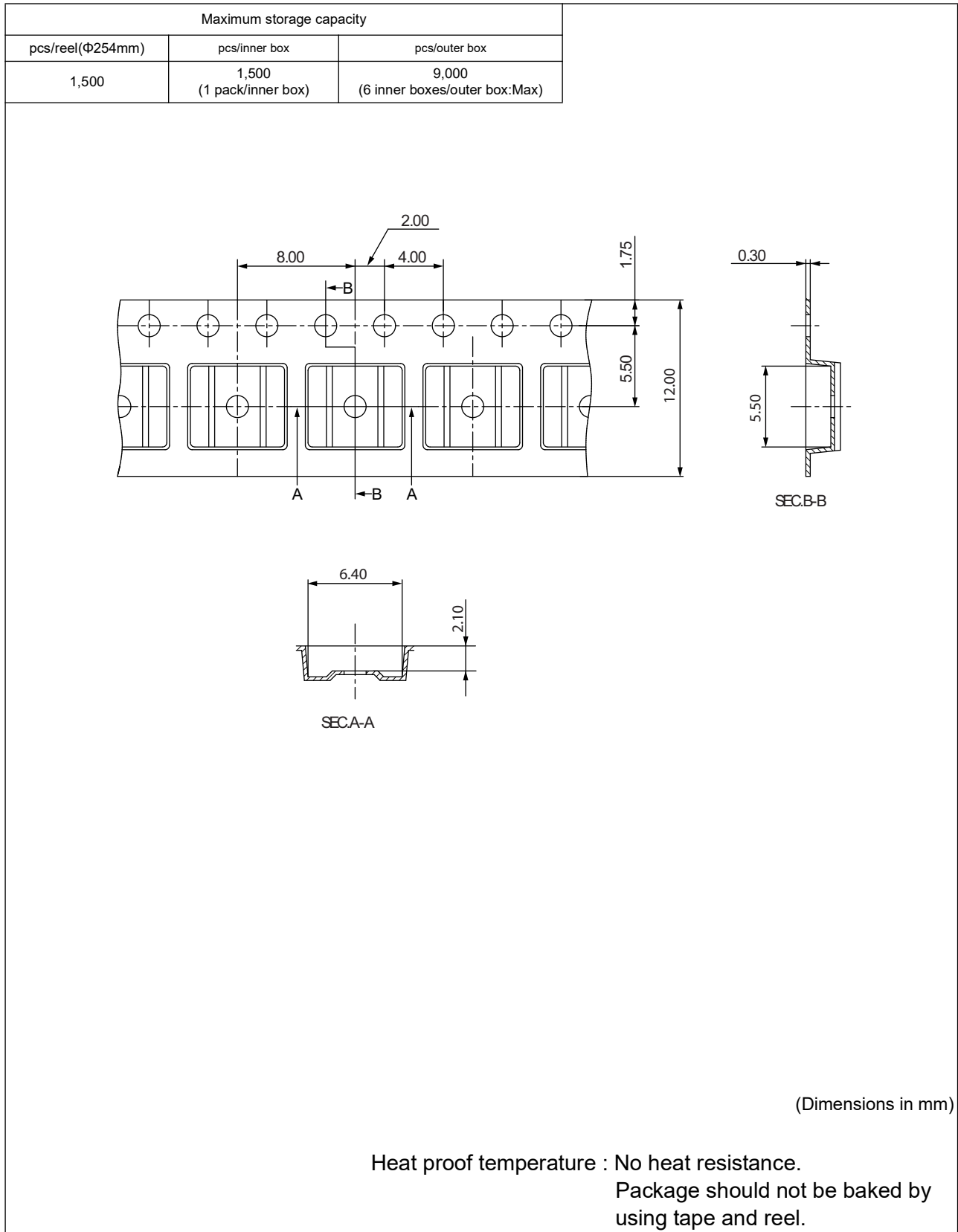


| L | W | H |
|-----|-----|-----|
| 565 | 270 | 180 |

(Dimensions in mm)

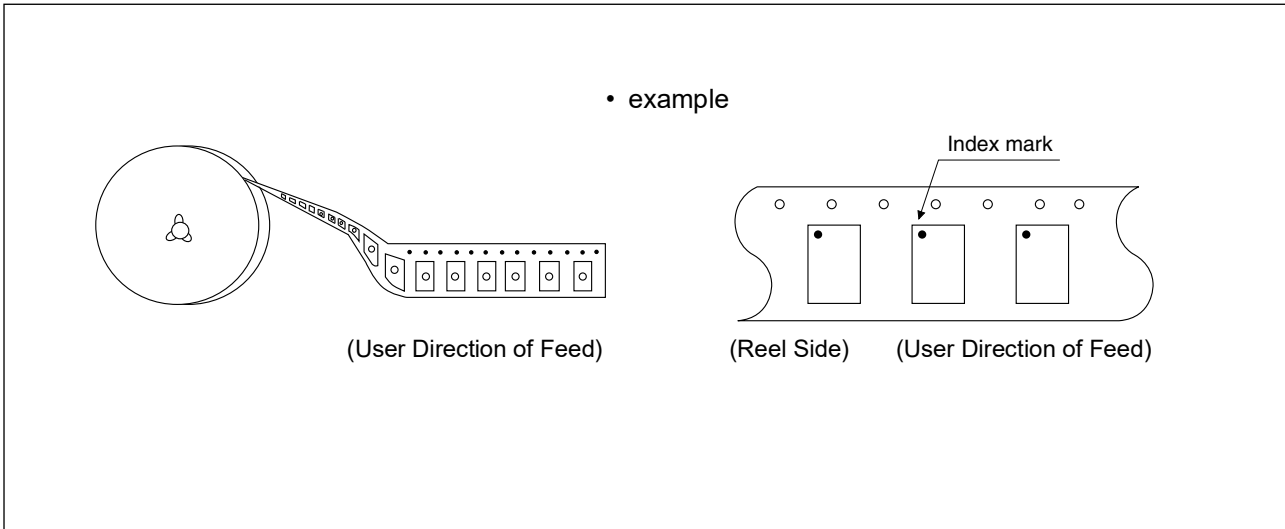
2. Emboss Tape (MB85RS256LYAPNF-G-BCERE1)

2.1 Tape Dimensions (not drawn to scale) (8-pin plastic SOP, 150mil)

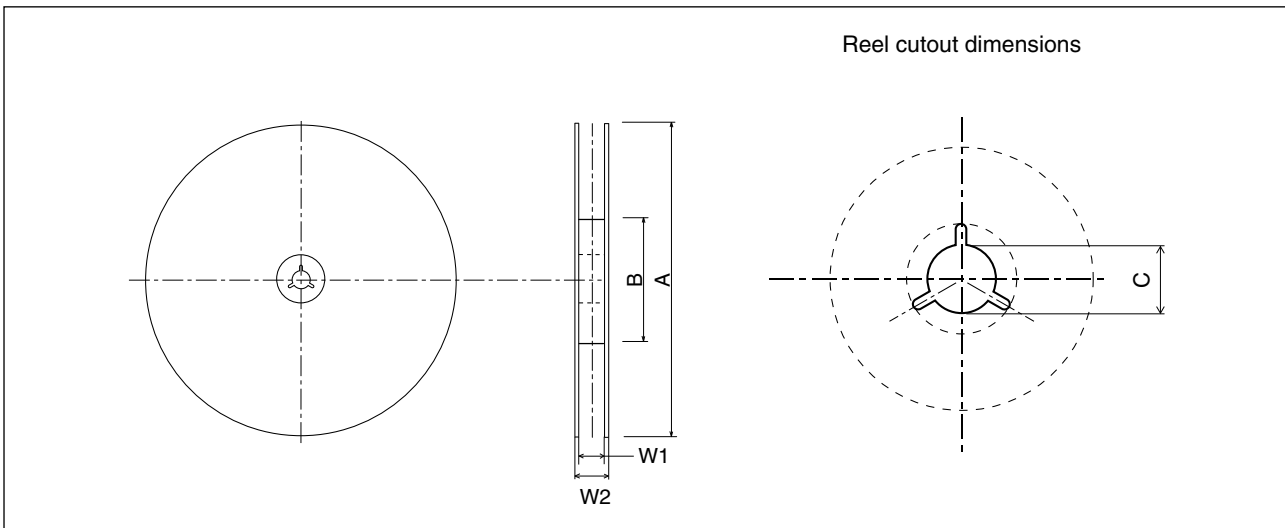


MB85RS256LYA

2.2 IC orientation



2.3 Reel dimensions



Dimensions in mm


| A | B | C | W1 | W2 |
|-----|-----|----|------|------|
| 254 | 100 | 13 | 13.5 | 17.5 |

2.4 Product label indicators (examples)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

| | |
|---|--|
| XXXXXXXXXXXXXXXX (Part number) (3N)1 XXXXXXXXXXXXXXXX XXX (LEAD FREE mark) (Part number and quantity) QC PASS (3N)2 XXXXXXXXXXXXXXXX XXXXXX (Control number bar code) XXX pcs (Quantity) XXXXXXXXXXXXXXXX (Part number) (Part number bar code) XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx XXXXXXXXXXXXXXXX (Part number) (Control number bar code) XX/XX (Package count) XXXX-XXX XXX XXXX-XXX XXX XXXXXXXXXXXXXXXX (Control number) (Lot Number and quantity) XXXXXXXXXXXXXXXX (Comment) | ← C-3 Label ← Perforated line ← Supplemental Label |
|---|--|

Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)
 [MSL Label]



Caution

This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
3

1. Calculated shelf life in sealed bag: 24 months at <40°C and <90% relative humidity (RH)
2. Peak package body temperature: 260°C
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
 - a) Mounted within: 168 hours of factory conditions <30°C/60% RH, or
 - b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
 - a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C
 - b) 3a or 3b are not met
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: see adjacent bar code label.

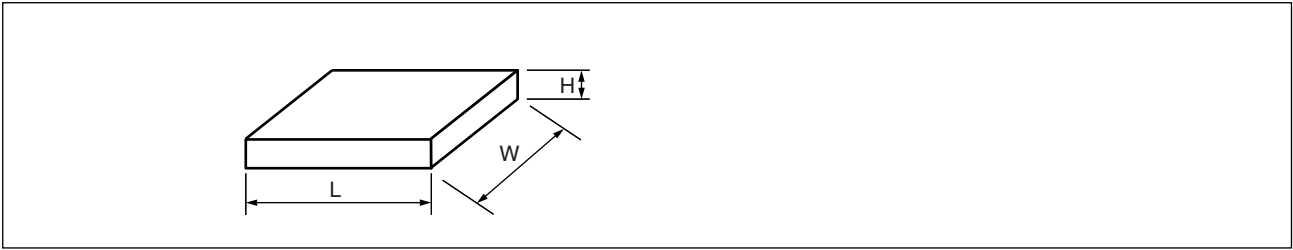
Note: Level and body temperature defined by IPC/JEDEC J-STD-020

← MSL label

MB85RS256LYA

2.5 Dimensions for Containers

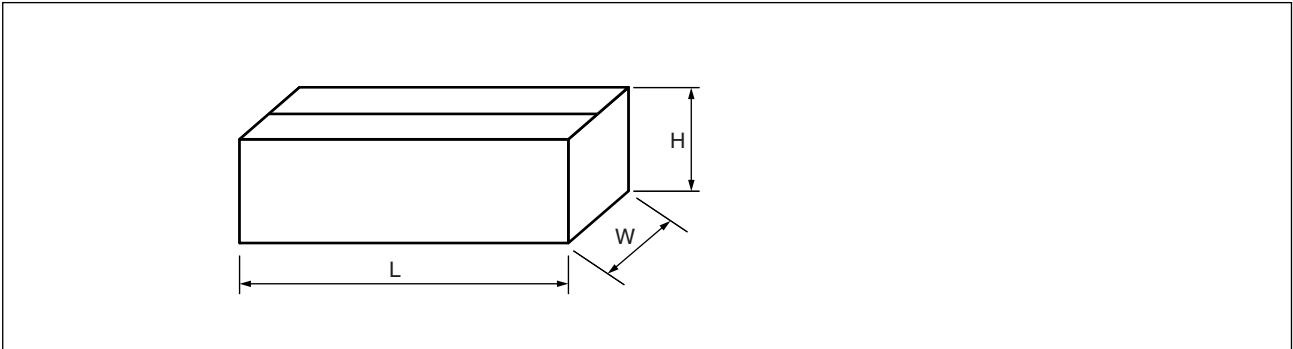
(1) Dimensions for inner box



| Tape width | L | W | H |
|------------|-----|-----|----|
| 12 | 265 | 260 | 50 |

(Dimensions in mm)

(2) Dimensions for outer box



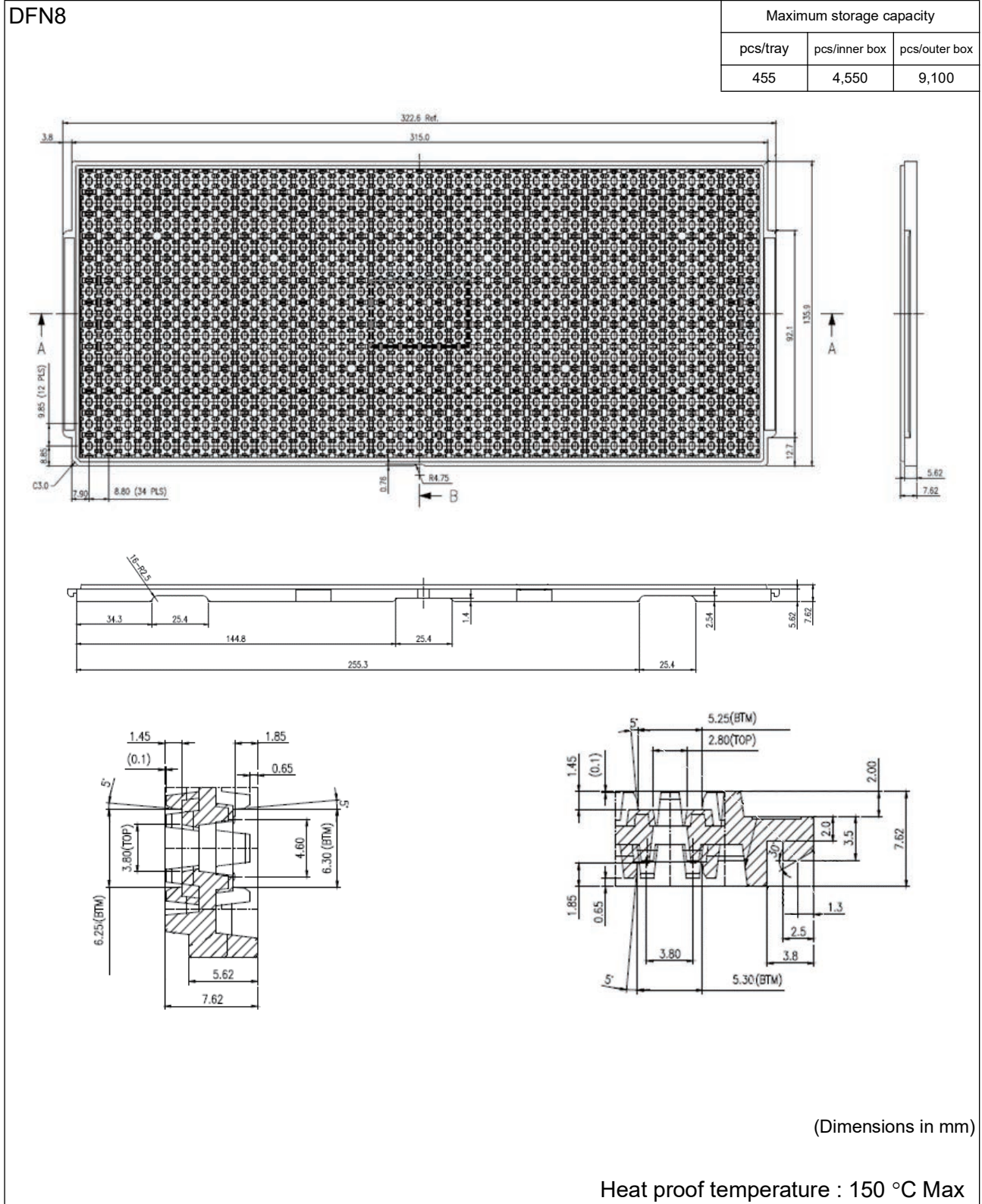
| L | W | H |
|-----|-----|-----|
| 565 | 270 | 180 |

(Dimensions in mm)

(2) MB85RS256LYAPN-G-AWE1/MB85RS256LYAPN-G-AWEWE1

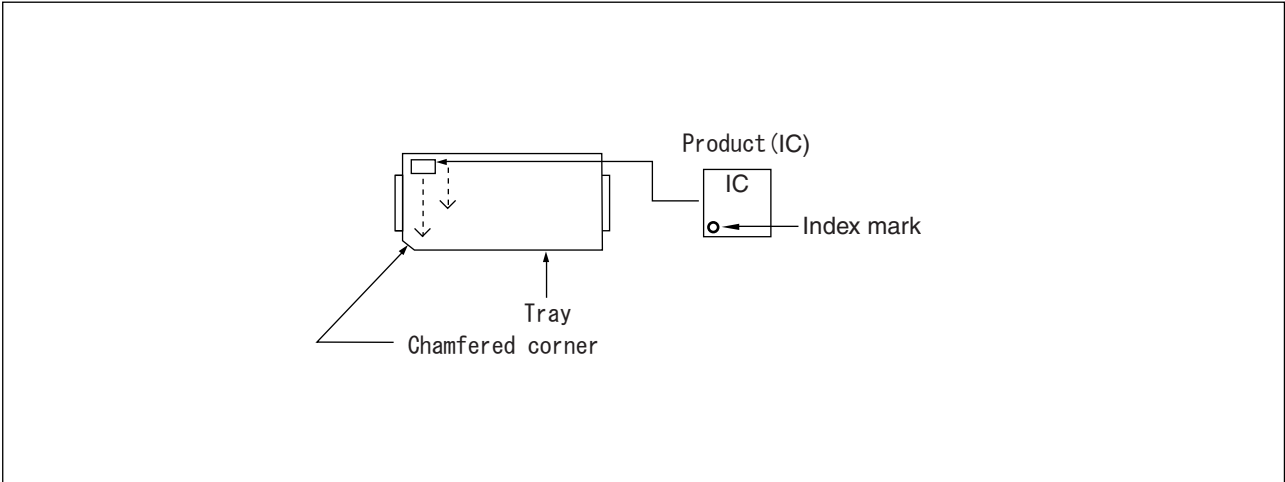
1. Tray (MB85RS256LYAPN-G-AWE1)

1.1 Tray Dimensions



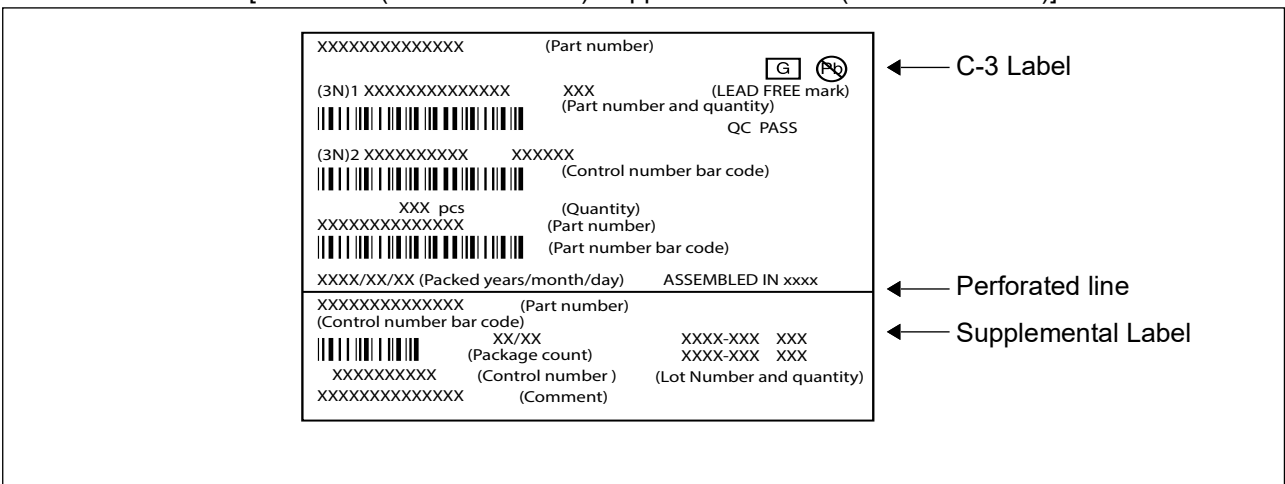
MB85RS256LYA

1.2 IC orientation



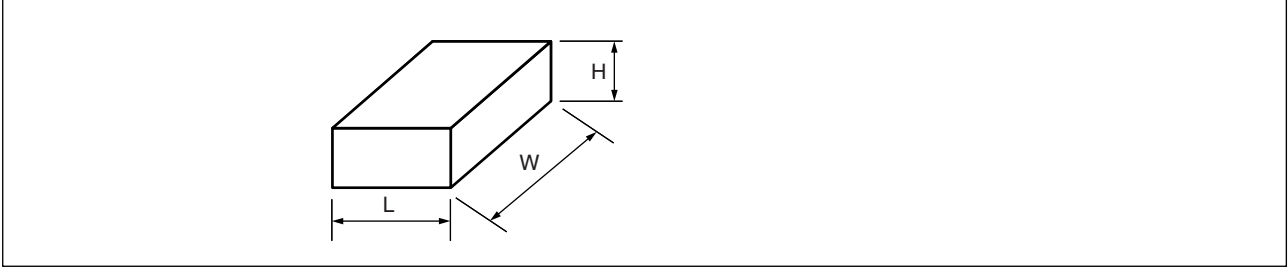
1.3 Product label indicators(example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



1.4 Dimensions for Containers

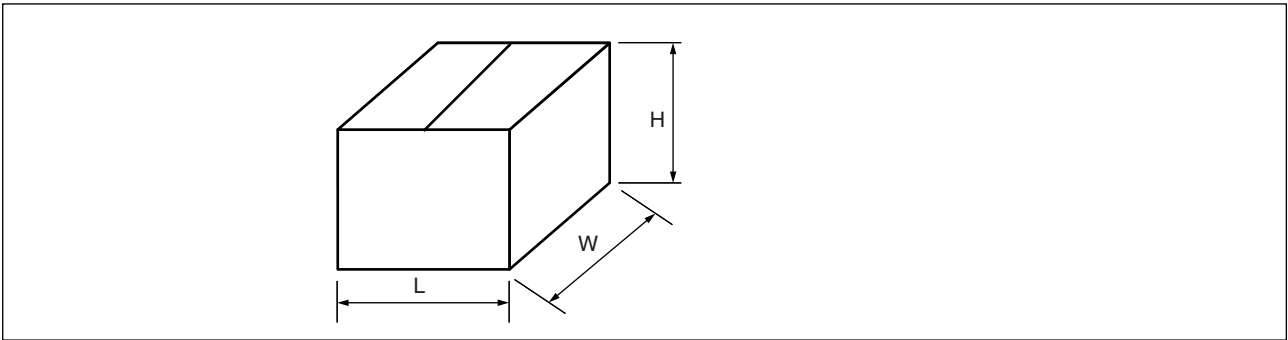
(1) Dimensions for inner box



| L | W | H |
|-----|-----|-----|
| 175 | 375 | 110 |

(Dimensions in mm)

(2) Dimensions for outer box



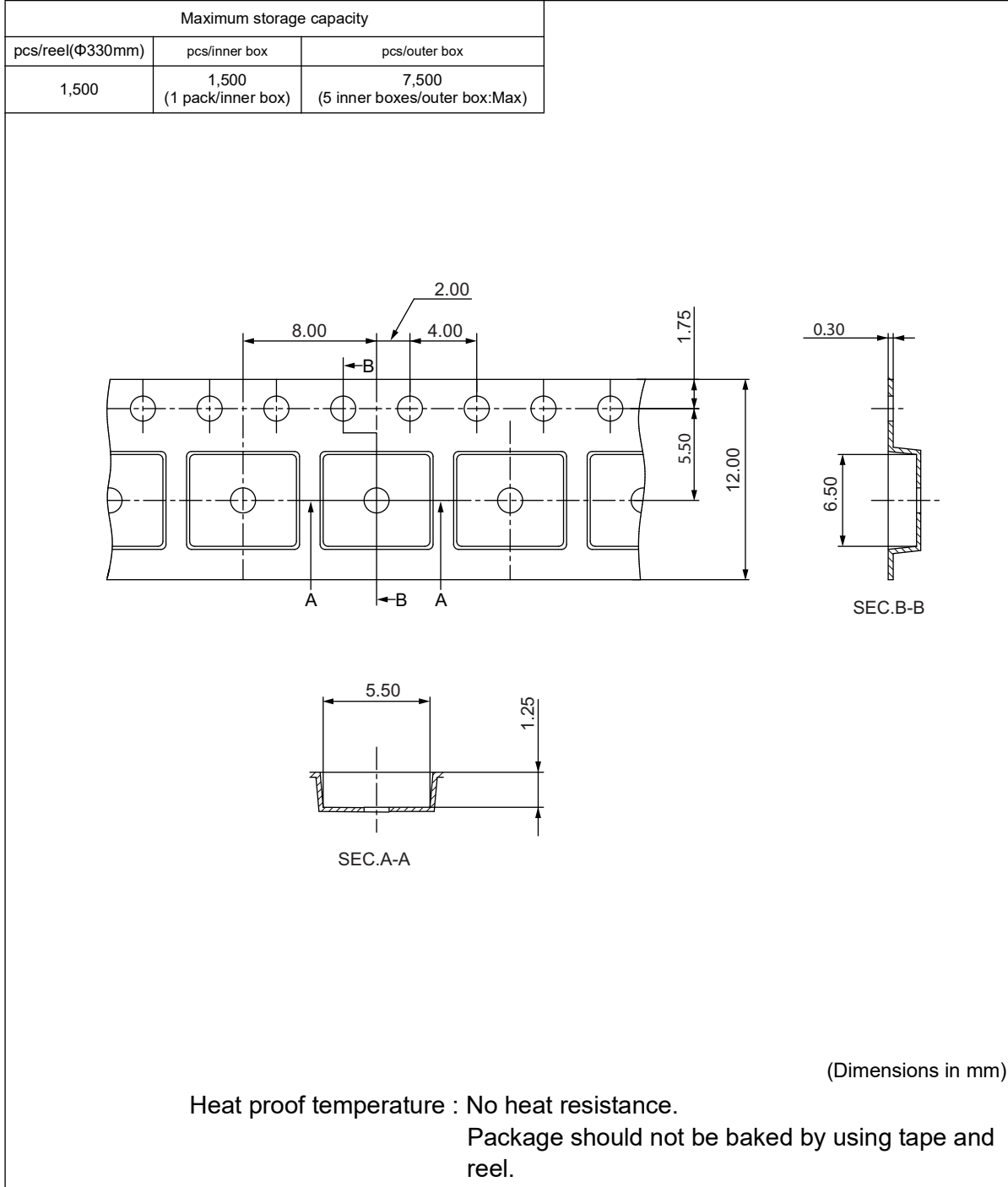
| L | W | H |
|-----|-----|-----|
| 190 | 380 | 330 |

(Dimensions in mm)

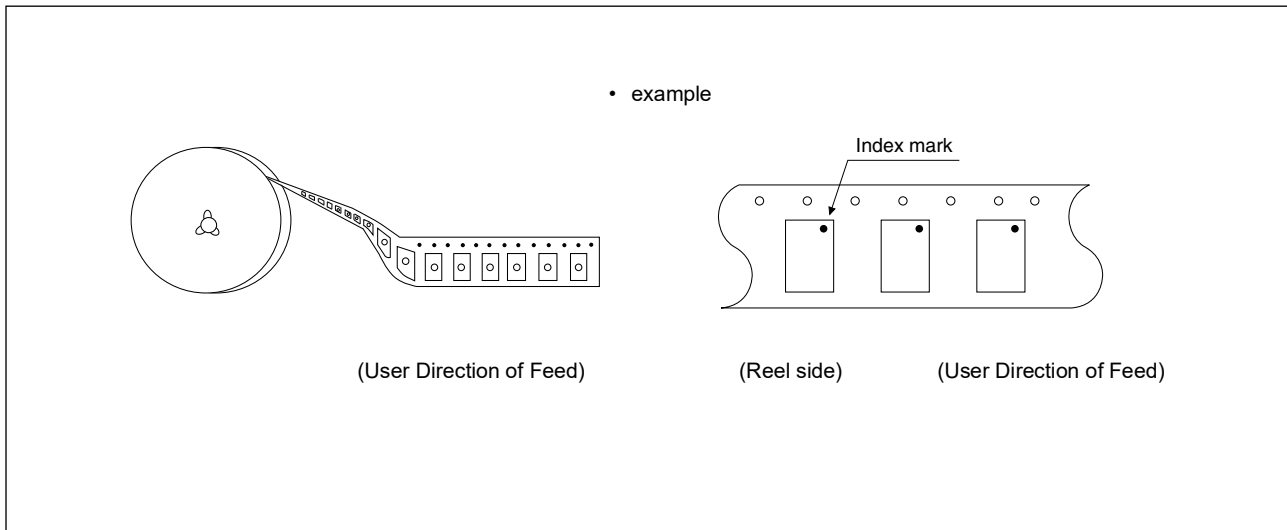
MB85RS256LYA

2. Emboss Tape (MB85RS256LYAPN-G-AWEWE1)

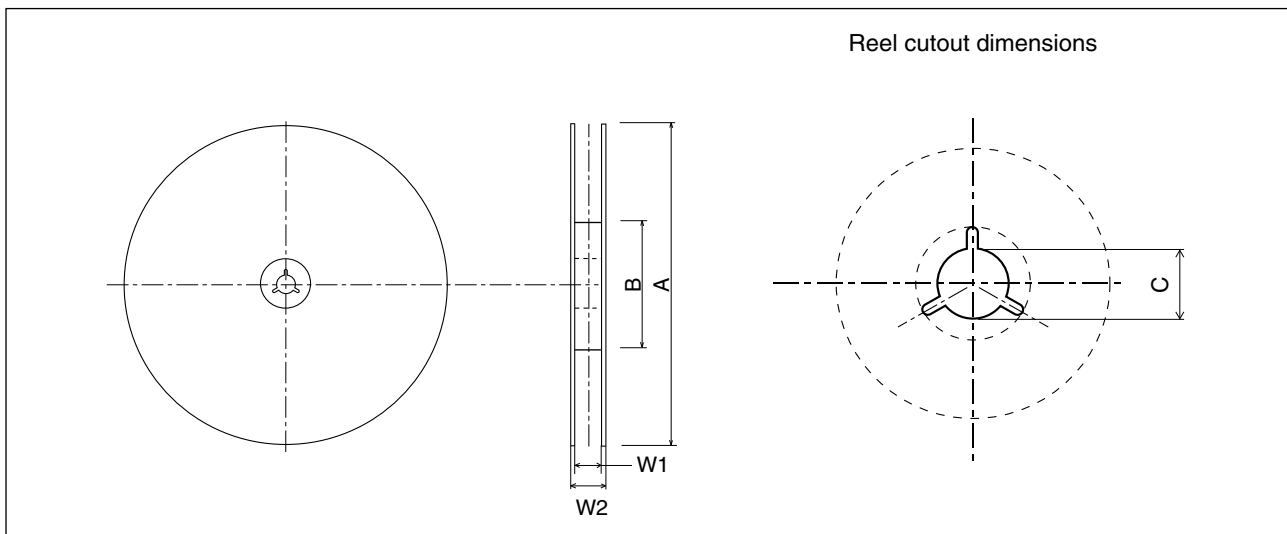
2.1 Tape Dimensions (not drawn to scale)(8-pin plastic DFN 5mm × 6mm)



2.2 IC orientation



2.3 Reel dimensions



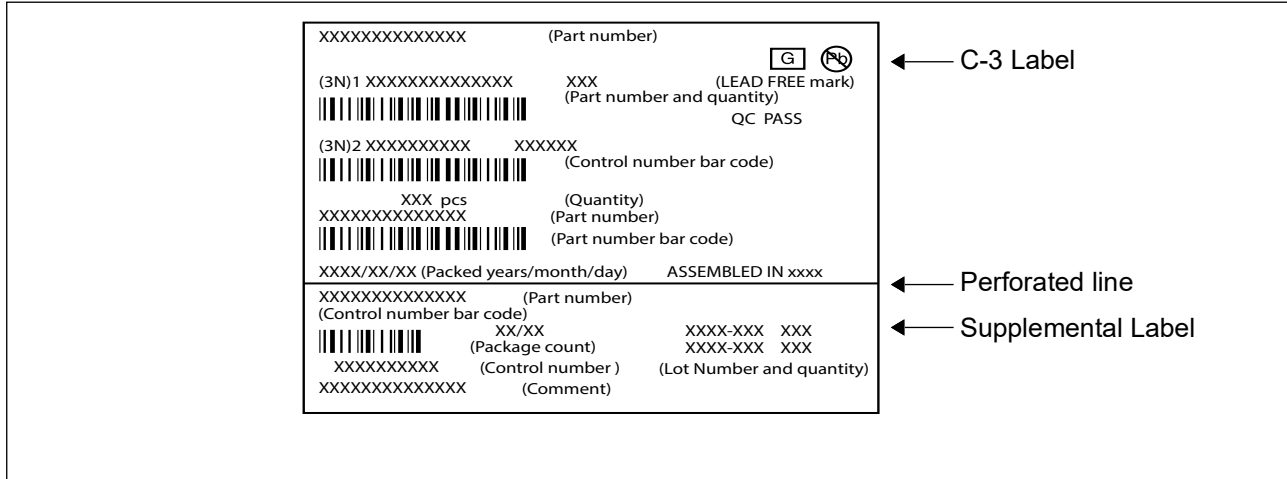
Dimensions in mm

| A | B | C | W1 | W2 |
|-----|-----|----|------|------|
| 330 | 100 | 13 | 13.5 | 17.5 |

MB85RS256LYA

2.4 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



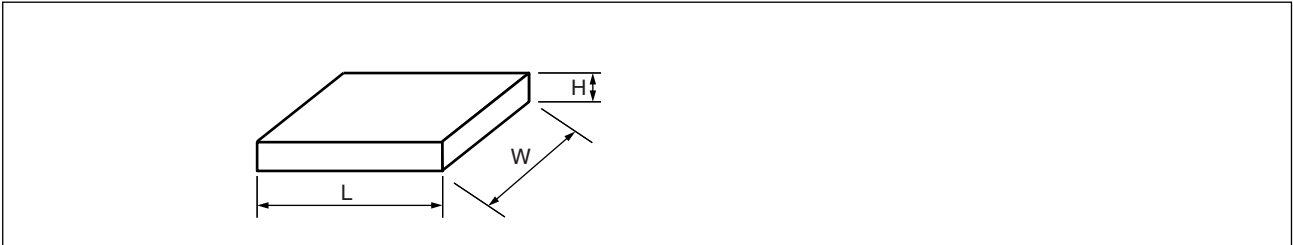
Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)

[MSL Label]



2.5 Dimensions for Containers

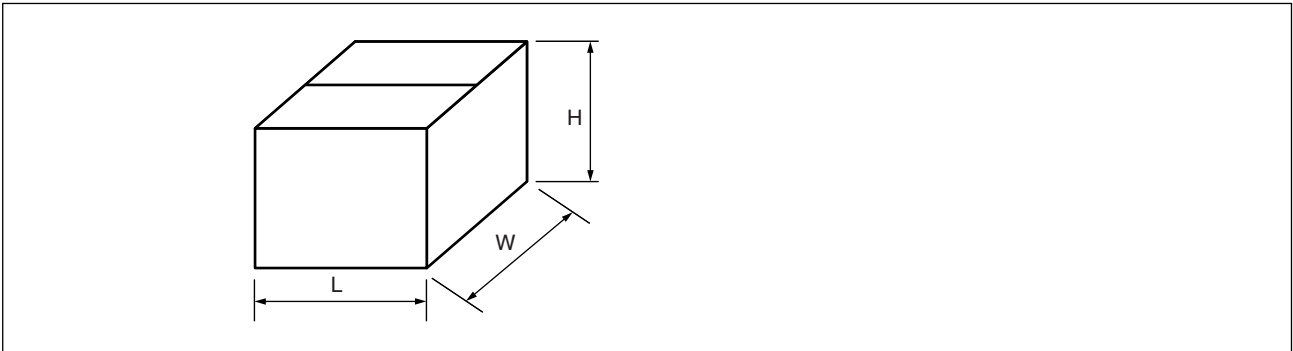
(1) Dimensions for inner box



| Tape width | L | W | H |
|------------|-----|-----|----|
| 12 | 350 | 335 | 35 |

(Dimensions in mm)

(2) Dimensions for outer box



| L | W | H |
|-----|-----|-----|
| 384 | 368 | 225 |

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn left side of that page.

| Page | Section | Change Results |
|------|----------------|--|
| 1,21 | Data Retention | 10.1 years(+125°C), 40.7 years(+105°C), 193.9 years(+85°C) |

MB85RS256LYA

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<https://ramxeed.com/>

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